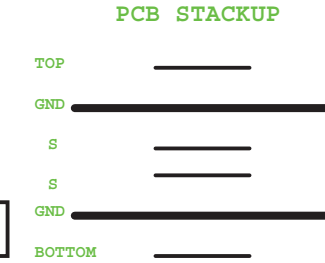
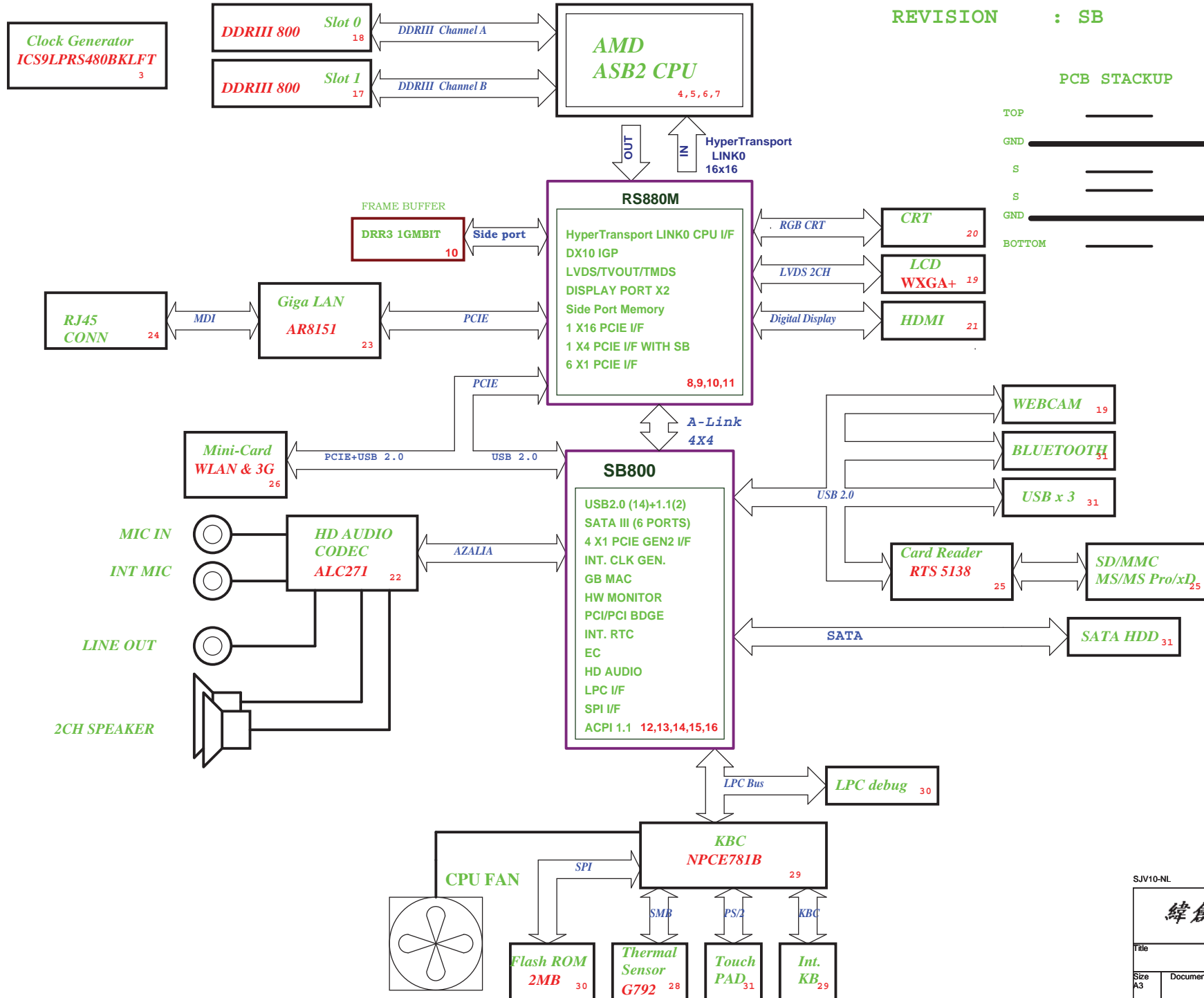


# JV10-NL Block Diagram

Project code: 91.4HX01.001  
PCB P/N : 48.4HX01.0SB  
REVISION : SB



SYSTEM DC/DC RT8223 34	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 (6A) 3D3V_S5 (6A)
SYSTEM DC/DC RT8209E 35	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 (7.5A)
SYSTEM DC/DC RT8209E 36	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0 (11A)
RT9026 35	
5V_S5	DDR_VREF_S3
RT9025 37	
3D3V_S5	1D1V_S5
RT9025 37	
3D3V_S5	CPU_VDDR
CHARGER ISL88731A 38	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA
CPU DC/DC ISL6265AHR 33	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

SJV10-NL

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Title Block Diagram	
Size A3	Document Number
SJV10-NL	
Date: Tuesday, January 05, 2010	Sheet 1 of 42
Rev -1	

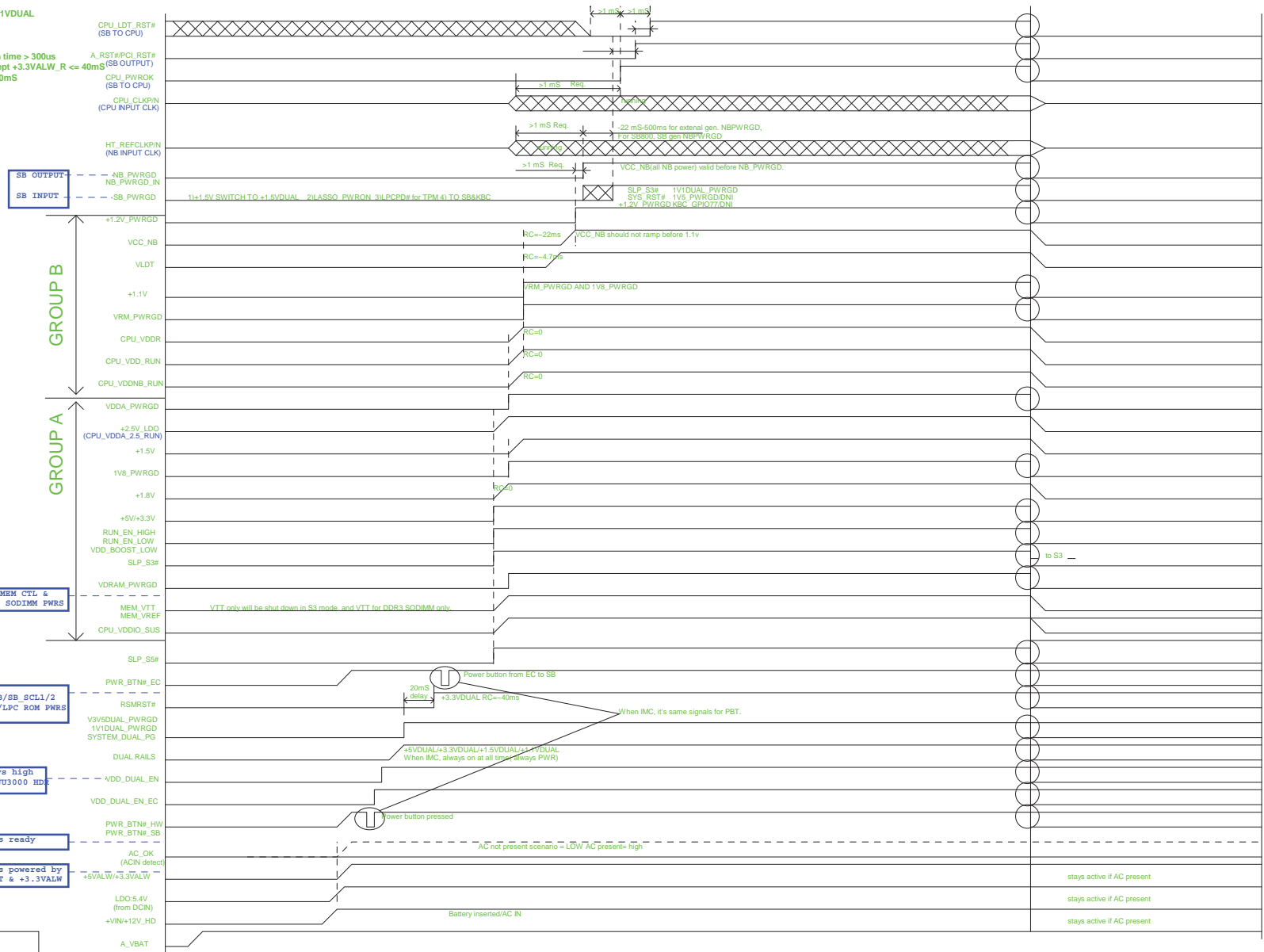
Power on Sequence required:

SB800:

- 1, +3.3VDUAL ramp before +1.1VDUAL
- 2, +3.3V ramp before +1.8V
- 3, +1.8V ramp before +1.1V
- 4, +3.3v ramp before +1.1V
- 5, +3.3VALW\_R ramping down time > 300us
- 6, 50uS <= All power rails except +3.3VALW\_R <= 40ms
- 7, 100uS <= +3.3VALW\_R <= 40mS

RS880:

- 1, 0 <(+3.3V) - (+1.8V) < 2.1
- 2, +1.8V ramp before +1.1V
- 3, +1.1V ramp before VCC\_NB



USB

Pair	Device
0	USB1 (HS)
1	MINICARD1
2	NC
3	NC
4	Cardreader
5	USB2
6	USB3
7	Blue Tooth
8	NC
9	WECCAM
10	NC
11	MINIC2 (3G sim)
12	MINIC2 (3G)
13	NC

## PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

SV10-NL

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Title

Table of Content

Size

Document Number

SV10-NL

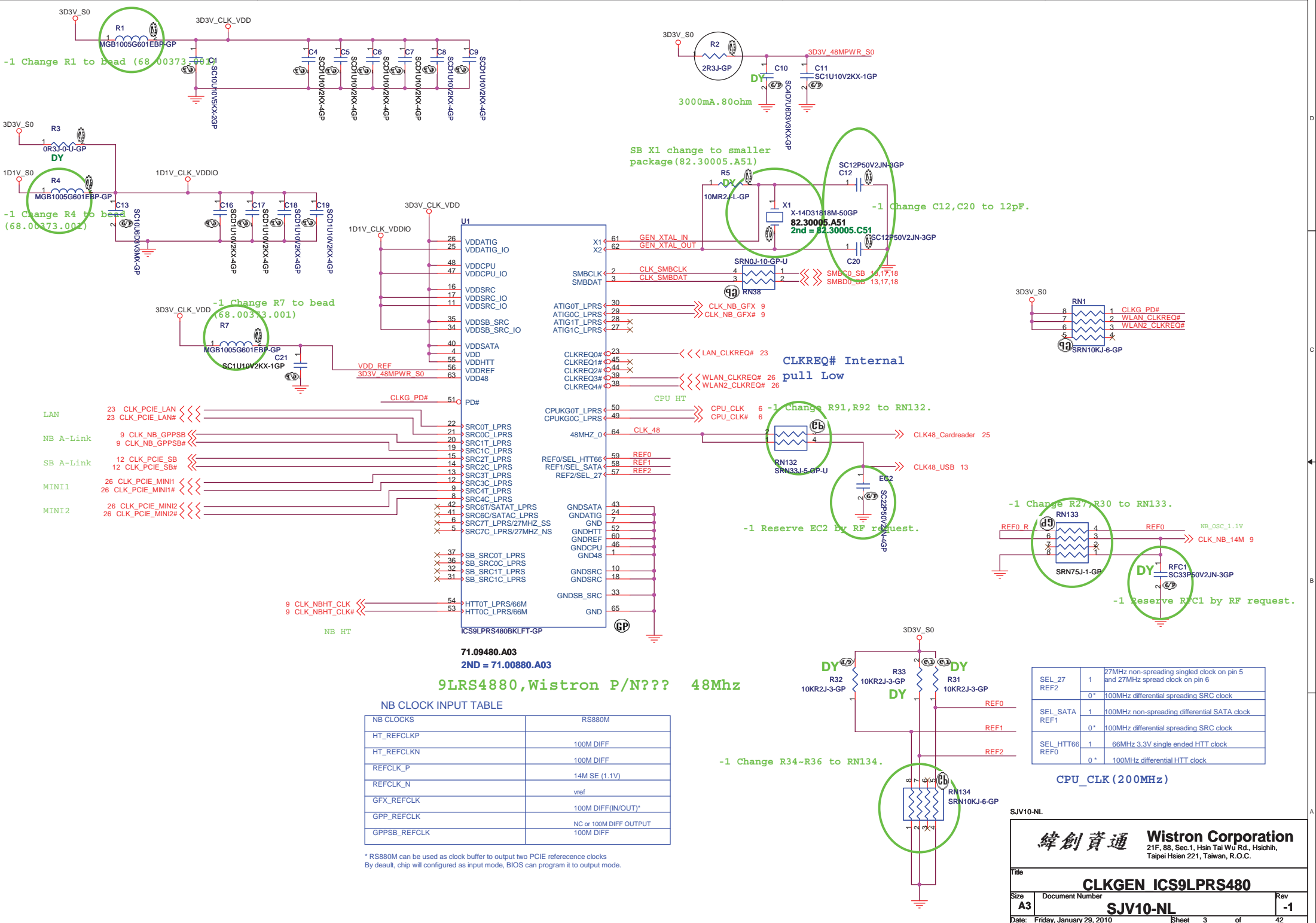
Rev

Date

Tuesday, January 05, 2010

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Rev -1



NB CLOCK INPUT TABLE

NB CLOCKS	RS880M
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	100M DIFF
REFCLK_N	14M SE (1.1V)
GFX_REFCLK	vref
GPP_REFCLK	100M DIFF(IN/OUT)*
GPPSB_REFCLK	NC or 100M DIFF OUTPUT
	100M DIFF

\* RS880M can be used as clock buffer to output two PCIe reference clocks  
By default, chip will configured as input mode, BIOS can program it to output mode.

SEL_27 REF2	1	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
	0*	100MHz differential spreading SRC clock
SEL_SATA REF1	1	100MHz non-spreading differential SATA clock
	0*	100MHz differential spreading SRC clock
SEL_HTT66 REF0	1	66MHz 3.3V single ended HTT clock
	0*	100MHz differential HTT clock

CPU\_CLK (200MHz)

SJV10-NL

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Title

CLKGEN ICS9LPRS480

Size

A3

Document Number

SJV10-NL

Rev

-1

Date

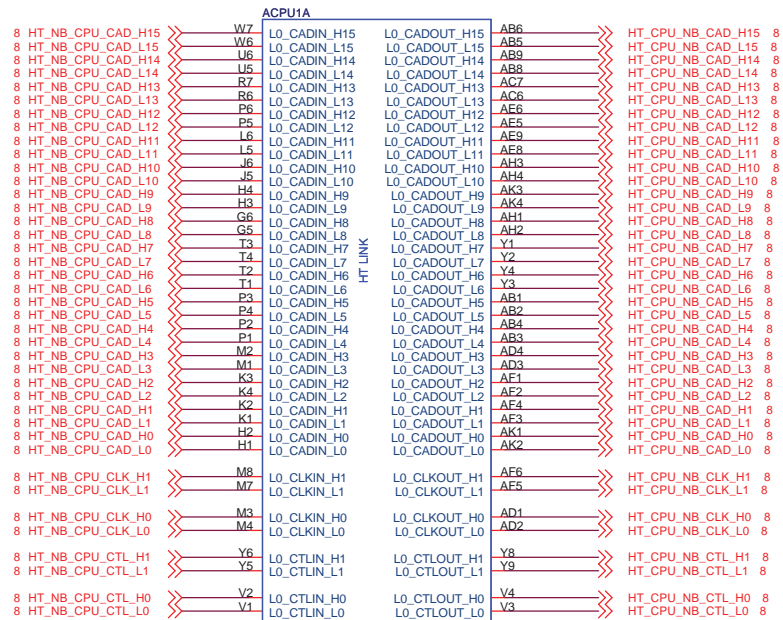
Friday, January 29, 2010

Sheet

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of

42



ASB2

71.TURON.B0U

SJV10-NL

緯創資通		Wistron Corporation	
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Title			
CPU HT LINK I/F (1/4)			
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A3	SJV10-NL	-1	
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17 M\_A\_DQ[63..0]  
17 M\_A\_A[15..0]  
17 M\_A\_DM[7..0]  
17 M\_A\_DQS#[7..0]  
17 M\_A\_DQS[7..0]

18 M\_B\_DQ[63..0]  
18 M\_B\_A[15..0]  
18 M\_B\_DM[7..0]  
18 M\_B\_DQS#[7..0]  
18 M\_B\_DQS[7..0]

# ACPU1B

M\_A A15 P30  
M\_A A14 M29  
M\_A A13 AG28  
M\_A A12 P28  
M\_A A11 T30  
M\_A A10 AC28  
M\_A A9 P27  
M\_A A8 R26  
M\_A A7 R27  
M\_A A6 U28  
M\_A A5 V30  
M\_A A4 U27  
M\_A A3 Y30  
M\_A A2 AB29  
M\_A A1 W29  
M\_A A0 AC26

17 M\_A\_BS2  
17 M\_A\_BS1  
17 M\_A\_BS0

MA\_ADD15  
MA\_ADD14  
MA\_ADD13  
MA\_ADD12  
MA\_ADD11  
MA\_ADD10  
MA\_ADD9  
MA\_ADD8  
MA\_ADD7  
MA\_ADD6  
MA\_ADD5  
MA\_ADD4  
MA\_ADD3  
MA\_ADD2  
MA\_ADD1  
MA\_ADD0  
MA\_BANK2  
MA\_BANK1  
MA\_BANK0  
MA\_CHECK7  
MA\_CHECK6  
MA\_CHECK5  
MA\_CHECK4  
MA\_CHECK3  
MA\_CHECK2  
MA\_CHECK1  
MA\_CHECK0  
MA\_DQS\_H8  
MA\_DQS\_L8  
MA\_DQS\_H7  
MA\_DQS\_L7  
MA\_DQS\_H6  
MA\_DQS\_L6  
MA\_DQS\_H5  
MA\_DQS\_L5  
MA\_DQS\_H4  
MA\_DQS\_L4  
MA\_DQS\_H3  
MA\_DQS\_L3  
MA\_DQS\_H2  
MA\_DQS\_L2  
MA\_DQS\_H1  
MA\_DQS\_L1  
MA\_DQS\_H0  
MA\_DQS\_L0  
MA\_CLK\_H7  
MA\_CLK\_L7  
MA\_CLK\_H6  
MA\_CLK\_L6  
MA\_CLK\_H5  
MA\_CLK\_L5  
MA\_CLK\_H4  
MA\_CLK\_L4  
MA\_CLK\_H3  
MA\_CLK\_L3  
MA\_CLK\_H2  
MA\_CLK\_L2  
MA\_CLK\_H1  
MA\_CLK\_L1  
MA\_CLK\_H0  
MA\_CLK\_L0  
MA\_DM8  
MA\_DM7  
MA\_DM6  
MA\_DM5  
MA\_DM4  
MA\_DM3  
MA\_DM2  
MA\_DM1  
MA\_DM0  
MA1\_ODT1  
MA1\_ODT0  
MA0\_ODT1  
MA0\_ODT0  
MA1\_CS\_L1  
MA1\_CS\_L0  
MA0\_CS\_L1  
MA0\_CS\_L0  
MA\_RAS\_L  
MA\_CAS\_L  
MA\_WE\_L  
MA\_RESET\_L  
FREE[MA\_EVENT\_L]

DDR III: CHANNEL A

GENEVA-GP

# ACPU1C

M\_B A15 P33  
M\_B A14 P31  
M\_B A13 A133  
M\_B A12 T32  
M\_B A11 T31  
M\_B A10 AD32  
M\_B A9 V32  
M\_B A8 U33  
M\_B A7 U33  
M\_B A6 V33  
M\_B A5 V31  
M\_B A4 W33  
M\_B A3 Y31  
M\_B A2 Y33  
M\_B A1 Y32  
M\_B A0 AC33

18 M\_B\_BS2  
18 M\_B\_BS1  
18 M\_B\_BS0

M\_B\_DQS7  
M\_B\_DQS#7  
M\_B\_DQS6  
M\_B\_DQS#6  
M\_B\_DQS5  
M\_B\_DQS#5  
M\_B\_DQS4  
M\_B\_DQS#4  
M\_B\_DQS3  
M\_B\_DQS#3  
M\_B\_DQS2  
M\_B\_DQS#2  
M\_B\_DQS1  
M\_B\_DQS#1  
M\_B\_DQS0  
M\_B\_DQS#0

18 M\_CLK\_DDR2  
18 M\_CLK\_DDR#2  
18 M\_CLK\_DDR#3

18 M\_CKE3  
18 M\_CKE2

18 M\_ODT3  
18 M\_ODT2

18 M\_CS#3  
18 M\_CS#2

18 M\_B\_RAS#  
18 M\_B\_CAS#  
18 M\_B\_WE#

18 DDR3\_DRAMRST\_B#  
17,18 PM\_EXTTS#1

MB\_ADD15  
MB\_ADD14  
MB\_ADD13  
MB\_ADD12  
MB\_ADD11  
MB\_ADD10  
MB\_ADD9  
MB\_ADD8  
MB\_ADD7  
MB\_ADD6  
MB\_ADD5  
MB\_ADD4  
MB\_ADD3  
MB\_ADD2  
MB\_ADD1  
MB\_ADD0  
MB\_BANK2  
MB\_BANK1  
MB\_BANK0  
MB\_CHECK7  
MB\_CHECK6  
MB\_CHECK5  
MB\_CHECK4  
MB\_CHECK3  
MB\_CHECK2  
MB\_CHECK1  
MB\_CHECK0  
MB\_DQS\_H8  
MB\_DQS\_L8  
MB\_DQS\_H7  
MB\_DQS\_L7  
MB\_DQS\_H6  
MB\_DQS\_L6  
MB\_DQS\_H5  
MB\_DQS\_L5  
MB\_DQS\_H4  
MB\_DQS\_L4  
MB\_DQS\_H3  
MB\_DQS\_L3  
MB\_DQS\_H2  
MB\_DQS\_L2  
MB\_DQS\_H1  
MB\_DQS\_L1  
MB\_DQS\_H0  
MB\_DQS\_L0  
MB\_CLK\_H7  
MB\_CLK\_L7  
MB\_CLK\_H6  
MB\_CLK\_L6  
MB\_CLK\_H5  
MB\_CLK\_L5  
MB\_CLK\_H4  
MB\_CLK\_L4  
MB\_CLK\_H3  
MB\_CLK\_L3  
MB\_CLK\_H2  
MB\_CLK\_L2  
MB\_CLK\_H1  
MB\_CLK\_L1  
MB\_CLK\_H0  
MB\_CLK\_L0  
MB\_CKE1  
MB\_CKE0  
MB1\_ODT1  
MB1\_ODT0  
MB0\_ODT1  
MB0\_ODT0  
MB1\_CS\_L1  
MB1\_CS\_L0  
MB0\_CS\_L1  
MB0\_CS\_L0  
MB\_RAS\_L  
MB\_CAS\_L  
MB\_WE\_L  
MB\_RESET\_L  
FREE[MB\_EVENT\_L]

DDR III: CHANNEL B

GENEVA-GP

SJV10-NL

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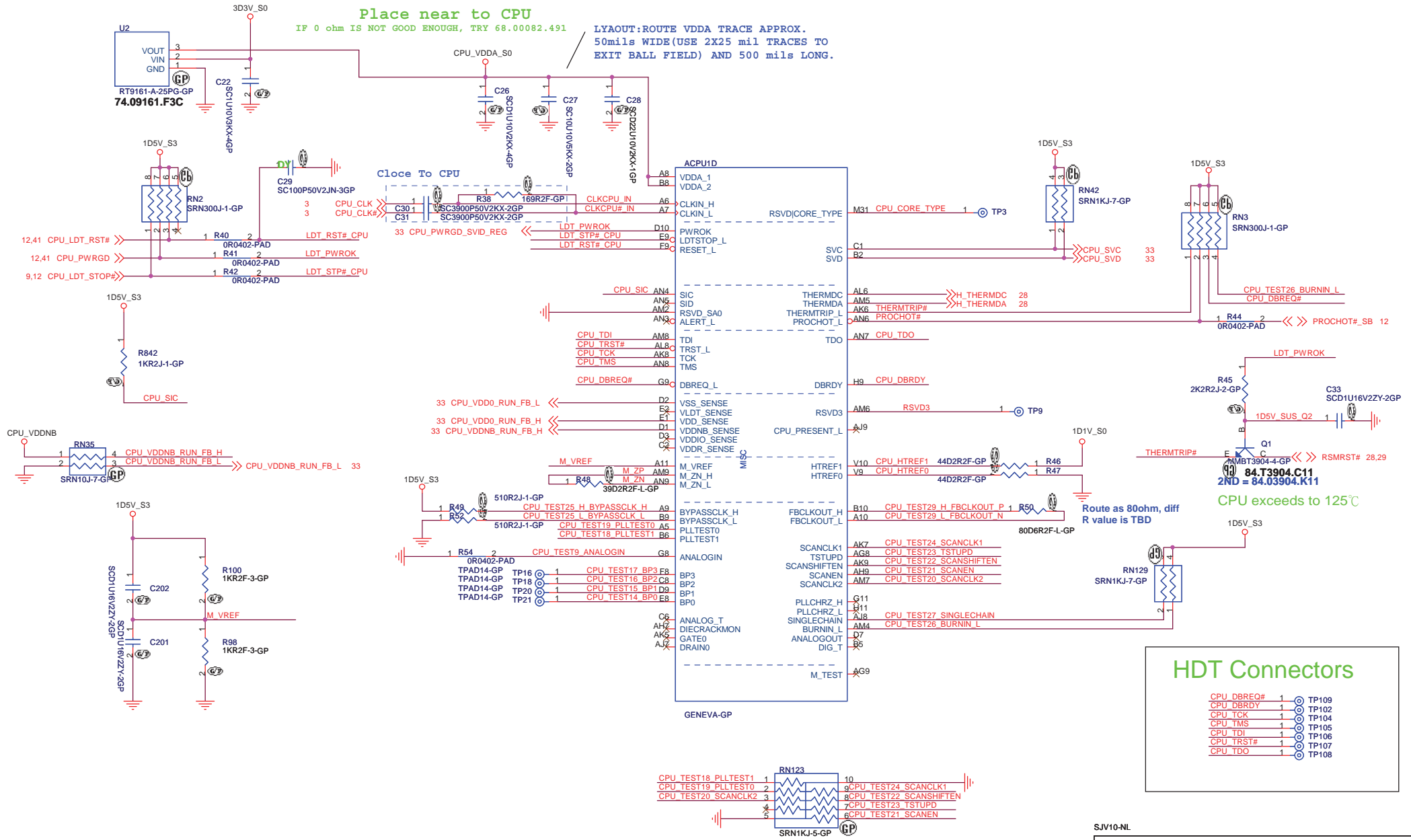
Title		
CPU DDR (2/4)		
Size	Document Number	Rev
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2D5V  
Iomax=0.2A

Place near to CPU

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX.  
50mils WIDE(USE 2X25 mil TRACES TO  
EXIT BALL FIELD) AND 500 mils LONG.



## HDT Connectors

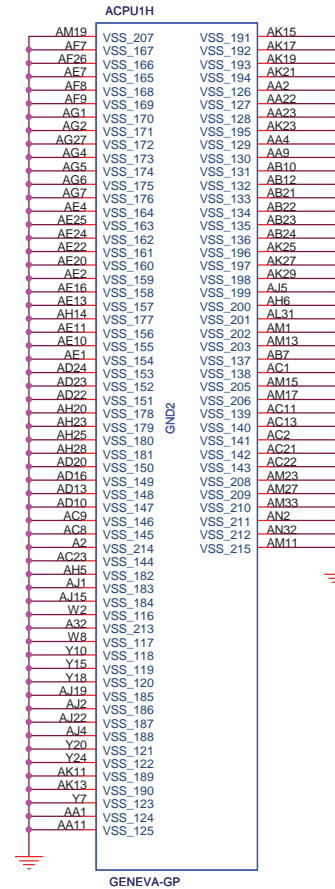
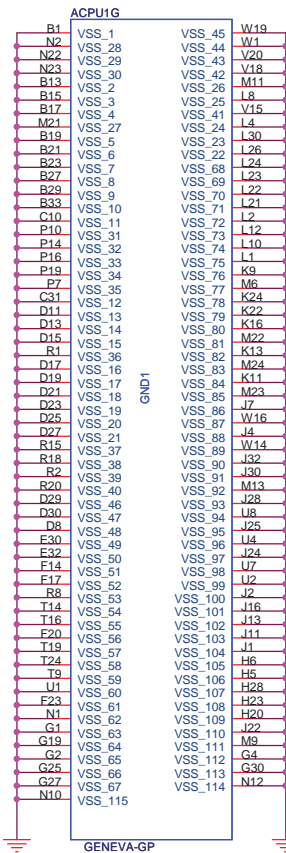
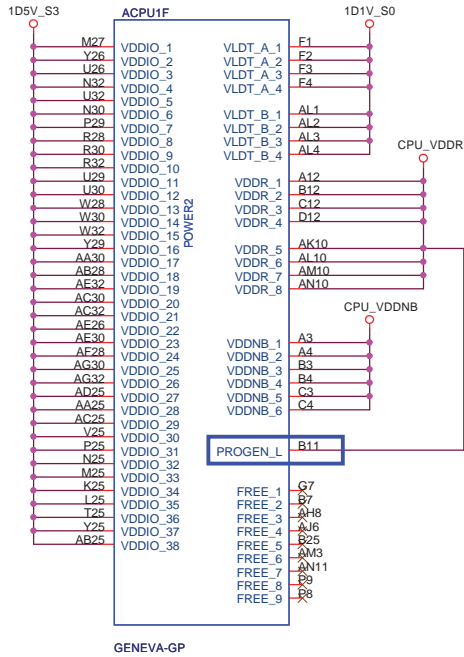
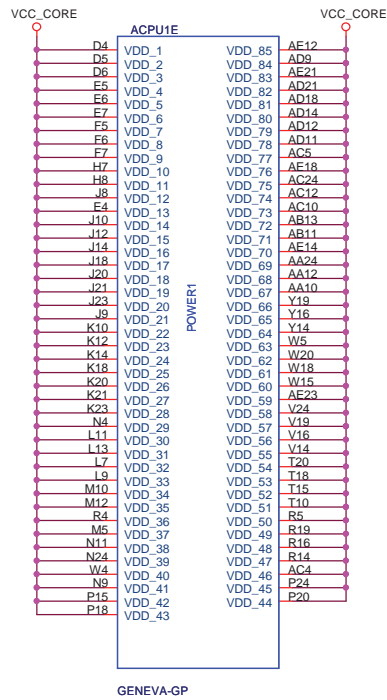
CPU DBREQ#	1	TP109
CPU DBRDY	1	TP102
CPU TCK	1	TP104
CPU TMS	1	TP105
CPU TDI	1	TP106
CPU TRST#	1	TP107
CPU TDO	1	TP108

SJV10-NL

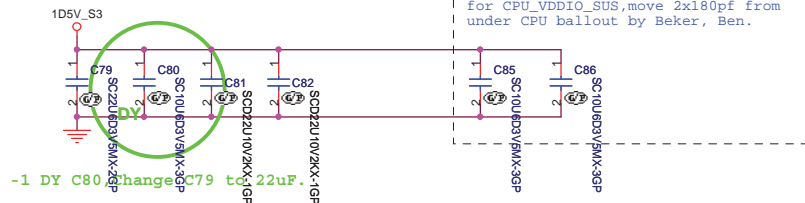
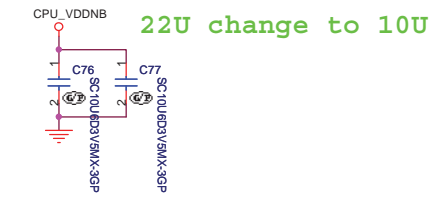
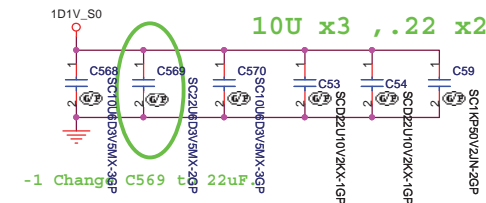
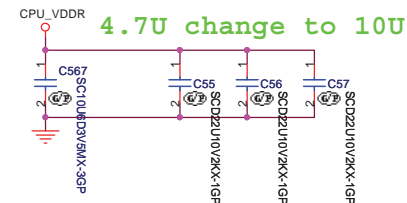
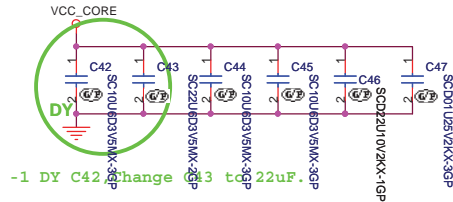
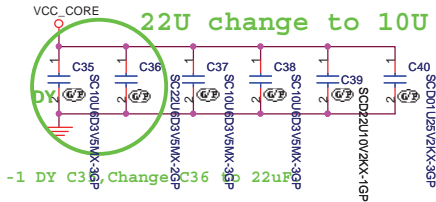
緯創資通 Wistron Corporation  
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Title CPU_Control&Debug_(3/4)		
Size A3	Document Number	Rev -1
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## BOTTOM SIDE DECOUPLING



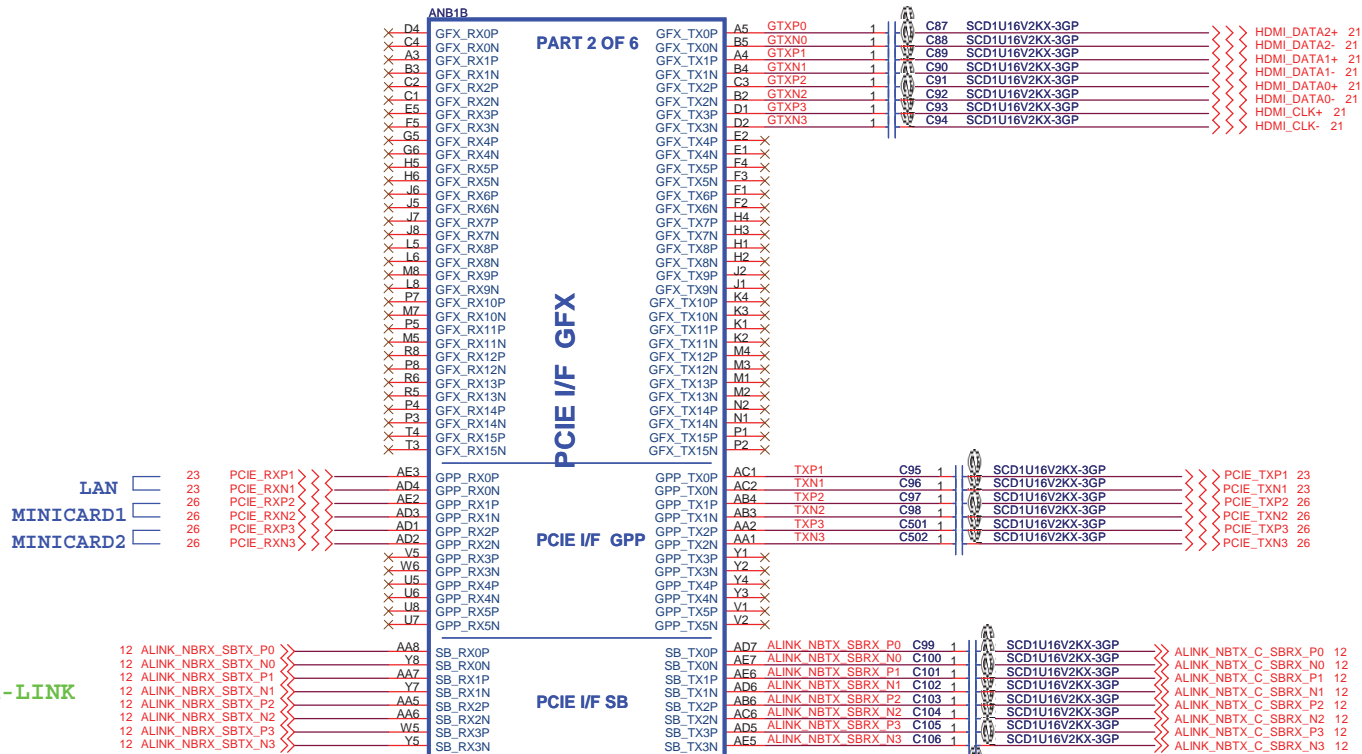
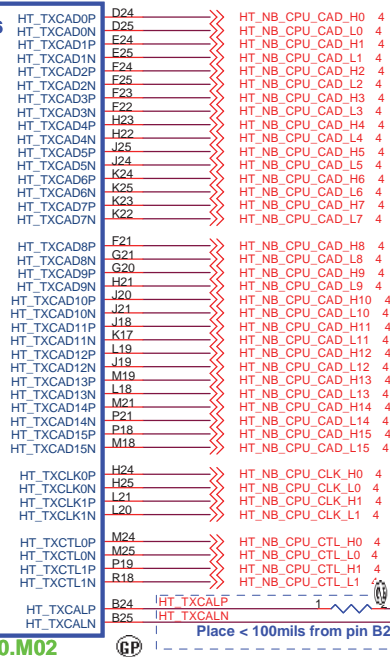
DECOUPLING between CPU and DIMMs  
PLACE CLOSE TO CPU AS POSSIBLE

It's required to add two 10uF/0603 size  
for CPU\_VDDIO\_SUS, move 2x180pf from  
under CPU ballout by Beker, Ben.

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Title			CPU_Power_(4/4)
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RS880M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

LAN  
MINICARD1  
MINICARD2

SJV10-NL

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Title		ATI-RS880M_HT LINK&PCle(1/4)	
Size	Document Number	Rev	
A3		-1	
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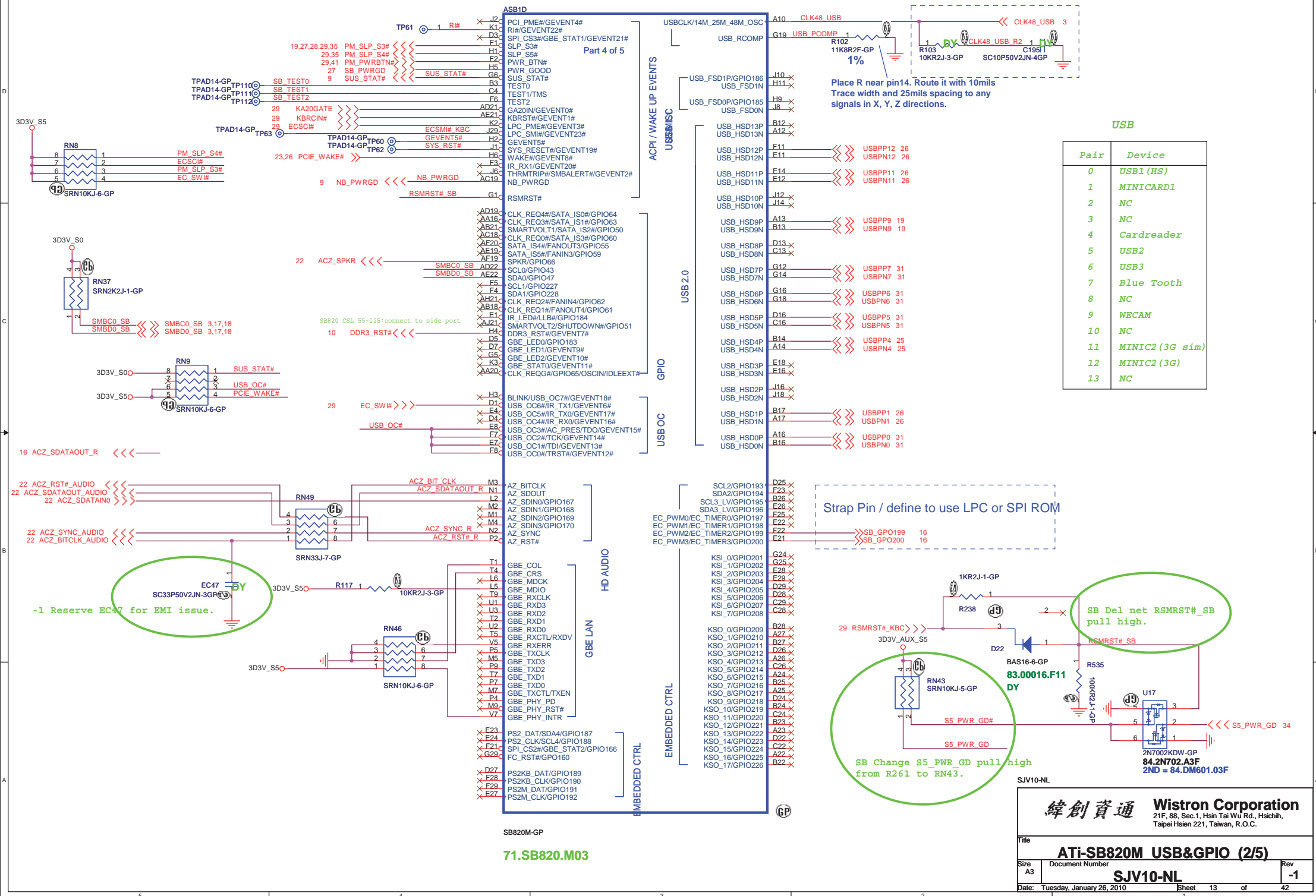




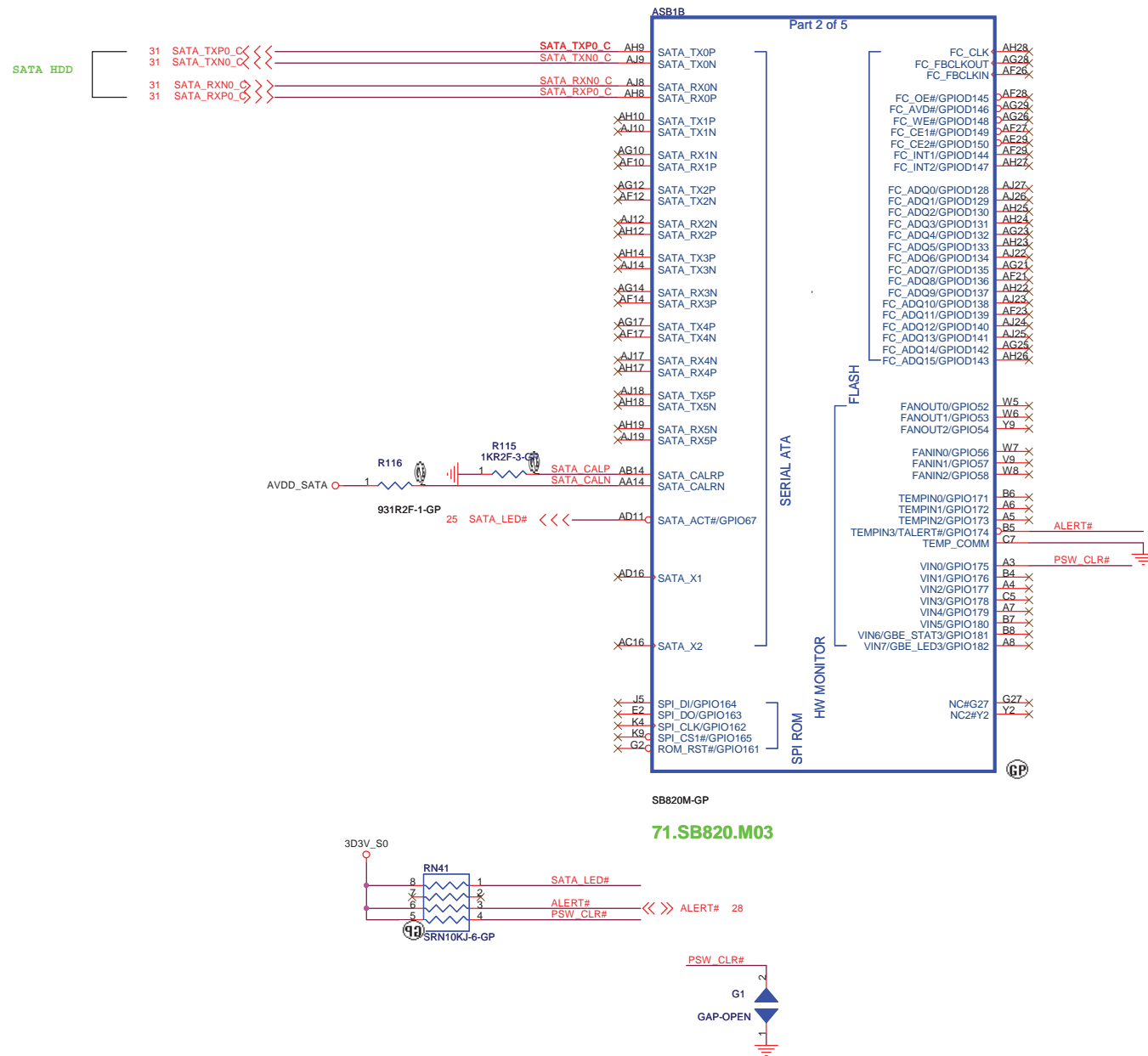








PLACE SATA AC DECOUPLING  
CAPS CLOSE TO SB710

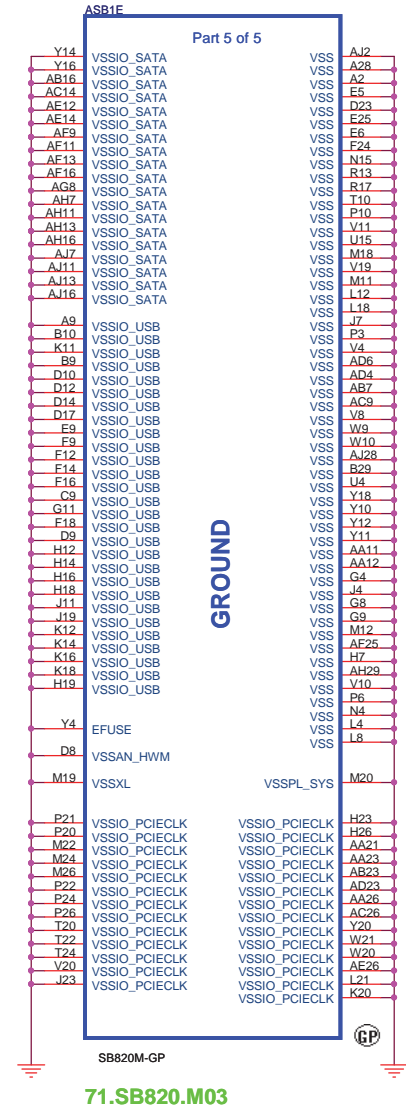
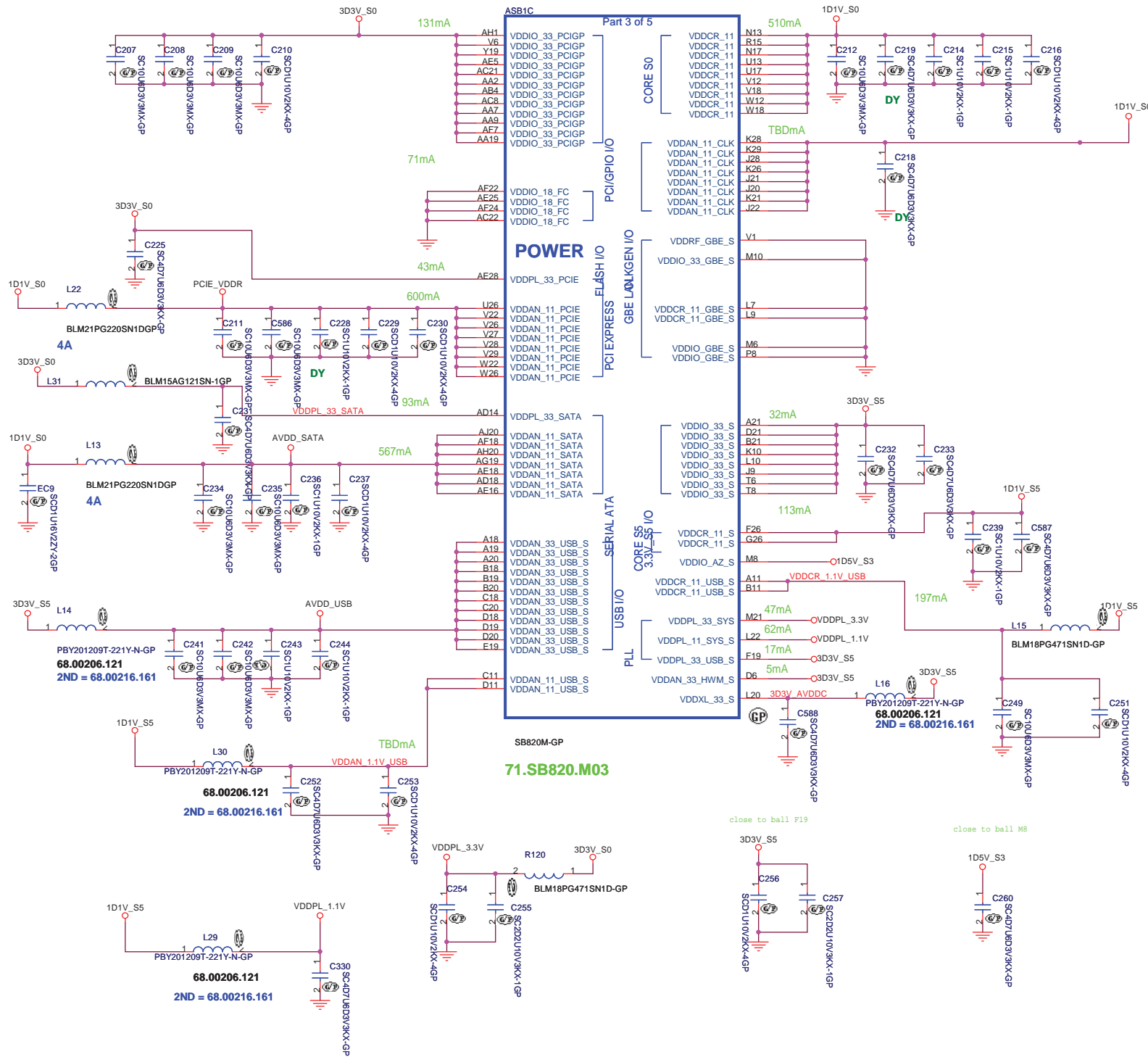


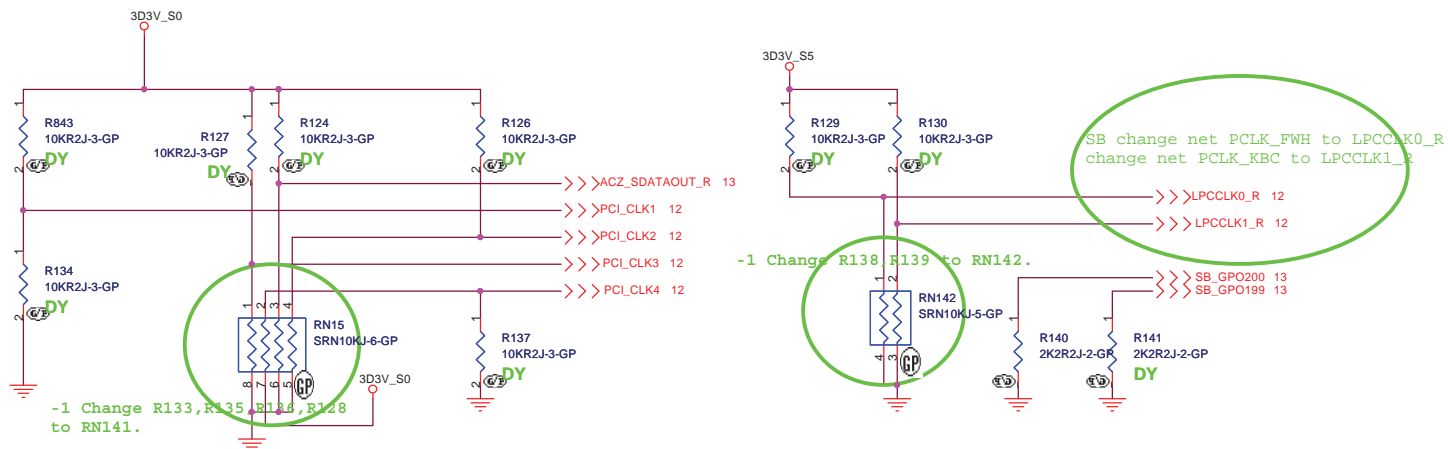
SJV10-NL

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Taipei Hsien 221, Taiwan, R.O.C.

Title		ATi-SB820M SATA-FC (3/5)	
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## REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM	

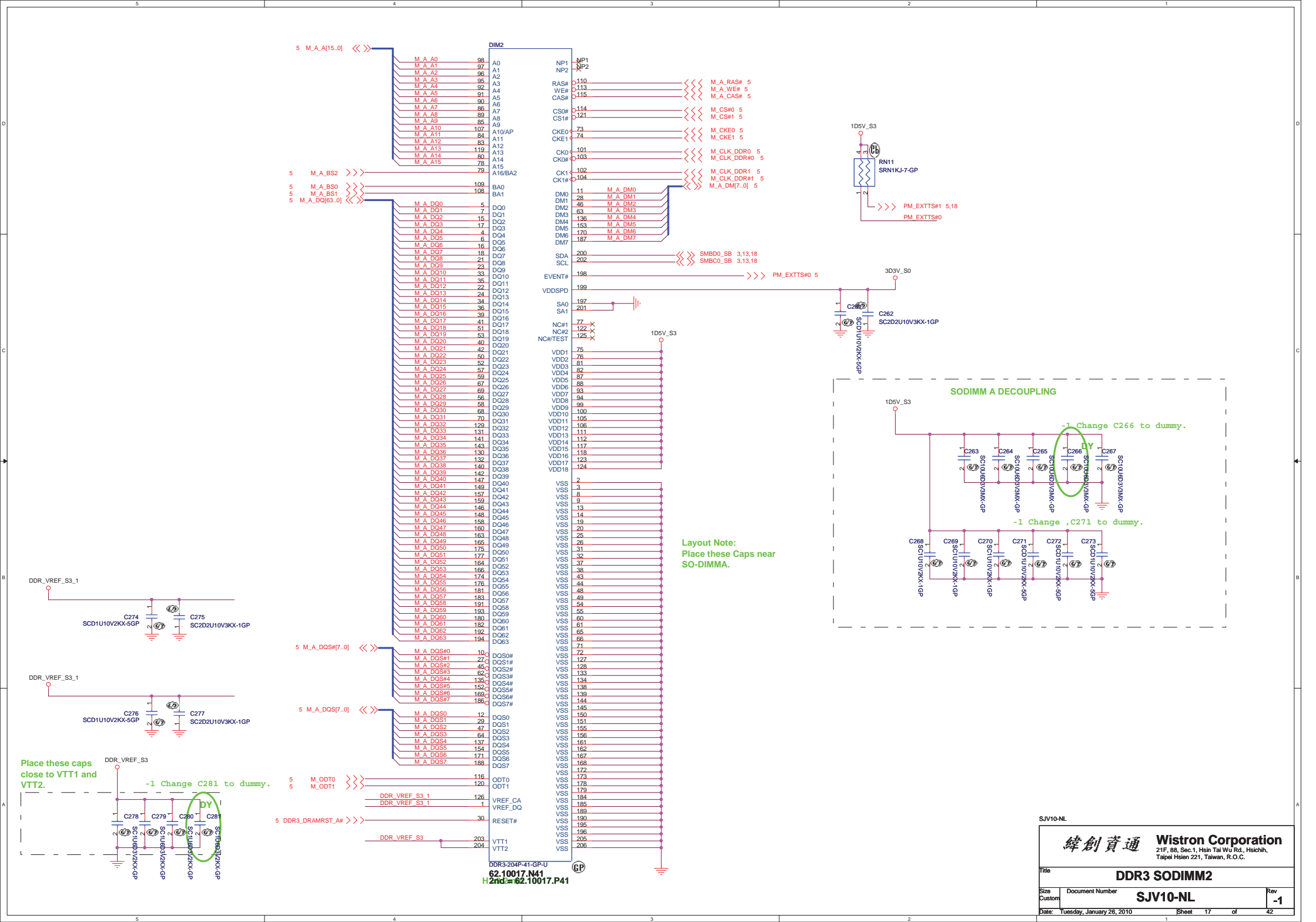
## DEBUG STRAPS

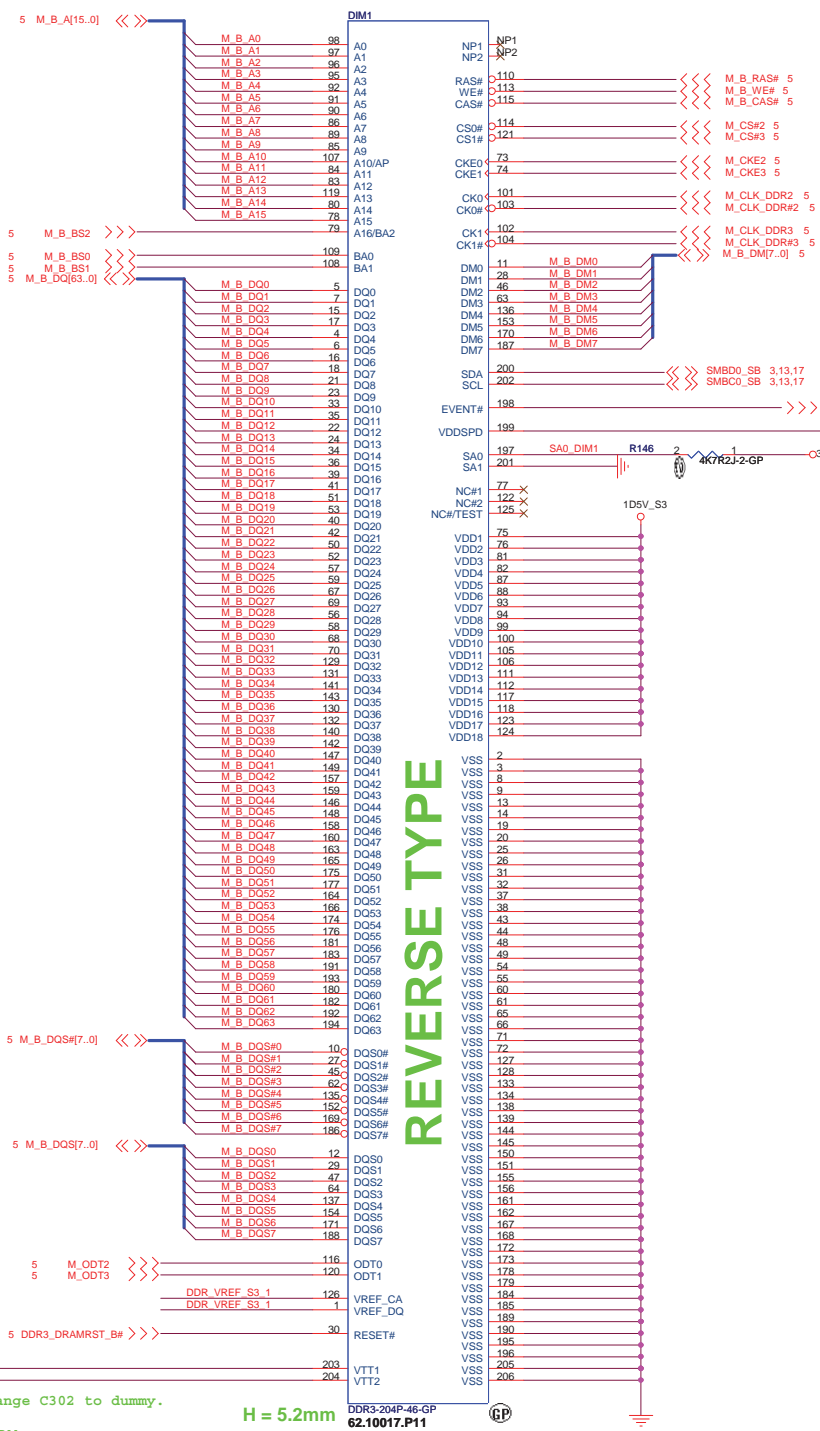
TPAD14-GP	TP79	PCI_AD23	12
TPAD14-GP	TP80	PCI_AD24	12
TPAD14-GP	TP81	PCI_AD25	12
TPAD14-GP	TP82	PCI_AD26	12
TPAD14-GP	TP83	PCI_AD27	12
TPAD14-GP	TP84	PCI_AD28	12
TPAD14-GP	TP85	PCI_AD29	12

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

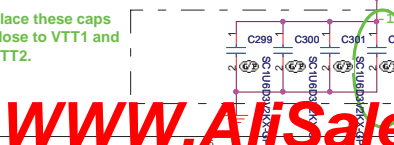
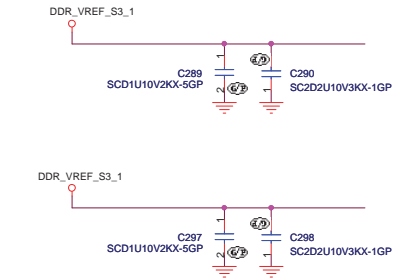
SJV10-NL

<b>緯創資通</b> <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
<b>ATI-SB820M STRAPPING (5/5)</b>	
Size	Document Number
A3	SJV10-NL
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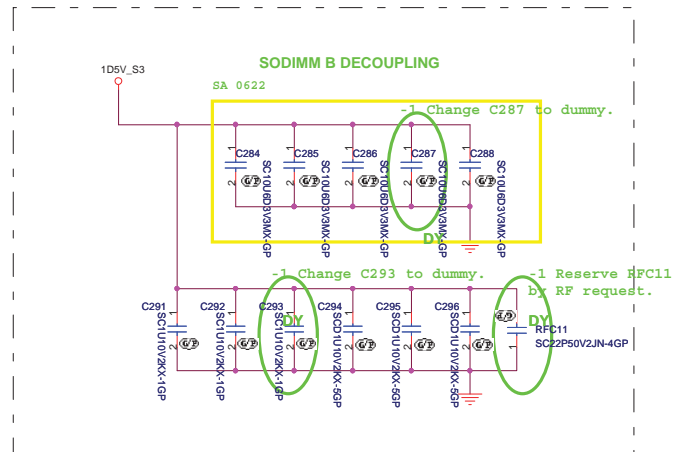


REVERSE TYPE



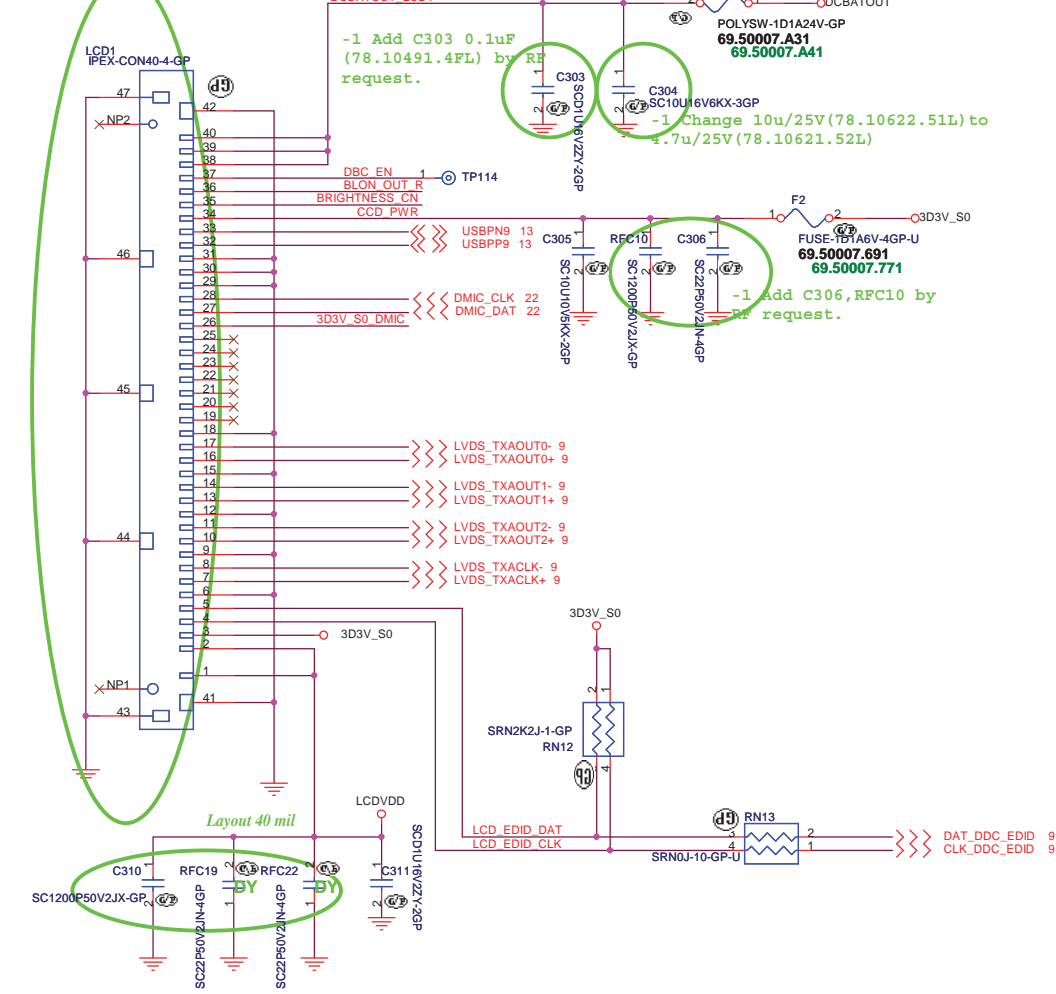
Note:  
SO-DIMMB SPD Address is 0xA4  
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from  
the Processor than SO-DIMMA



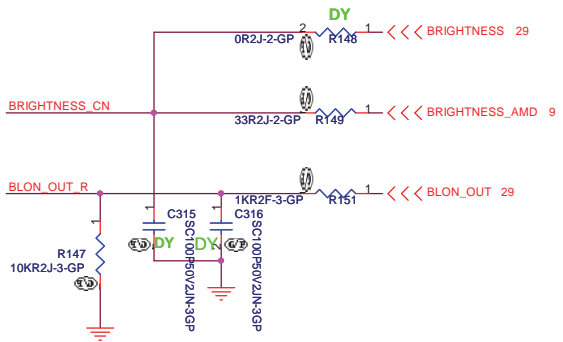
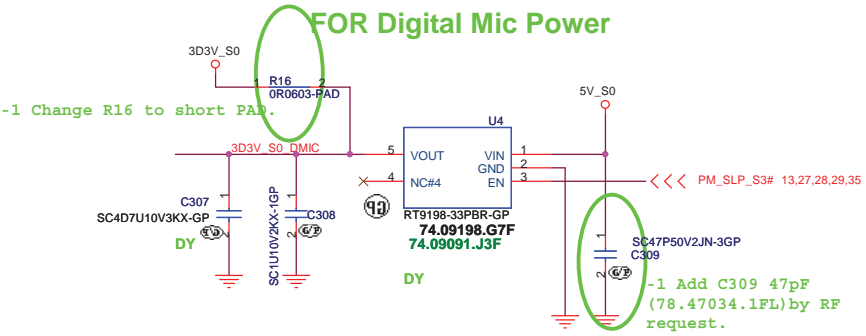
SJV10-NL	
緯創資通 Wistron Corporation	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File	
DDR3 SODIMM1	
Size	Document Number
Custom	SJV10-NL
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SB Change P/N from 20.F1093.040  
to 20.F1703.040

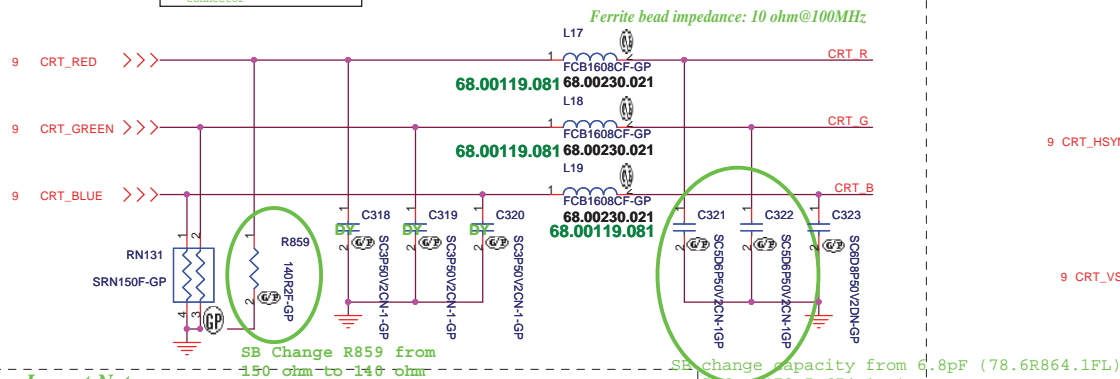


CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	NC

D MIC Pin	
Pin	Symbol
1	DMIC_DAT
2	3D3V_S0_DMIC
3	DMIC_CLK
4	GND



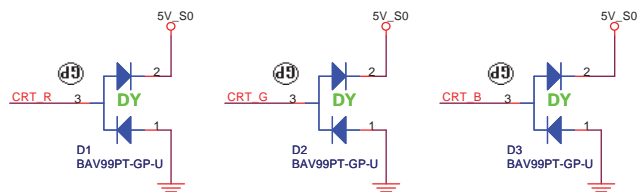
Layout Note:  
Place these resistors  
close to the CRT-out  
connector



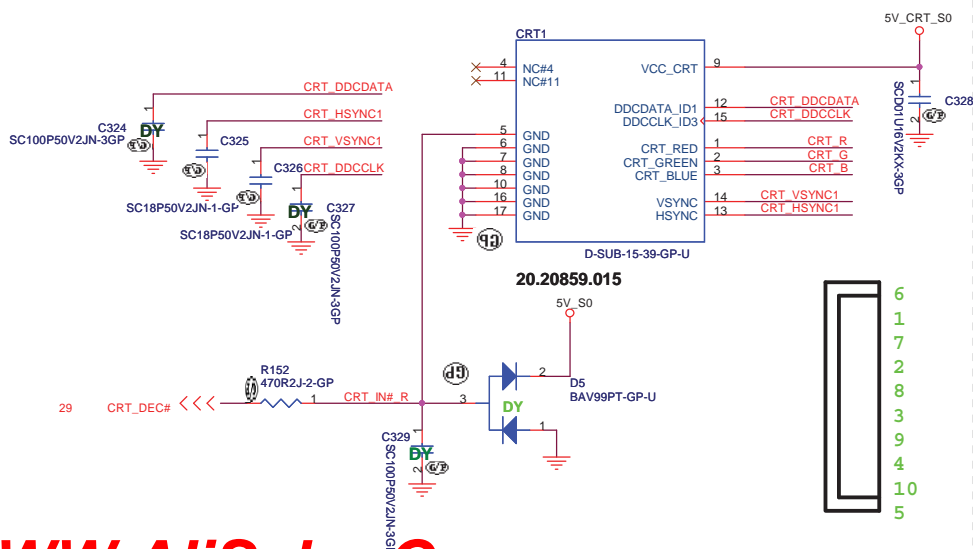
Layout Note:

\* Must be a ground return path between this ground and the ground on the VGA connector.

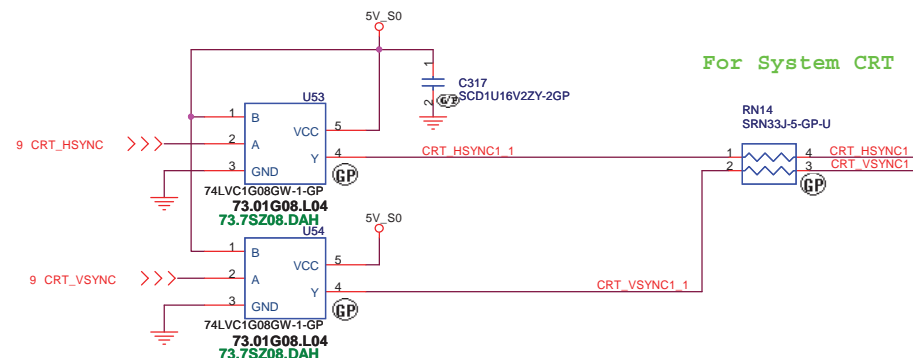
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



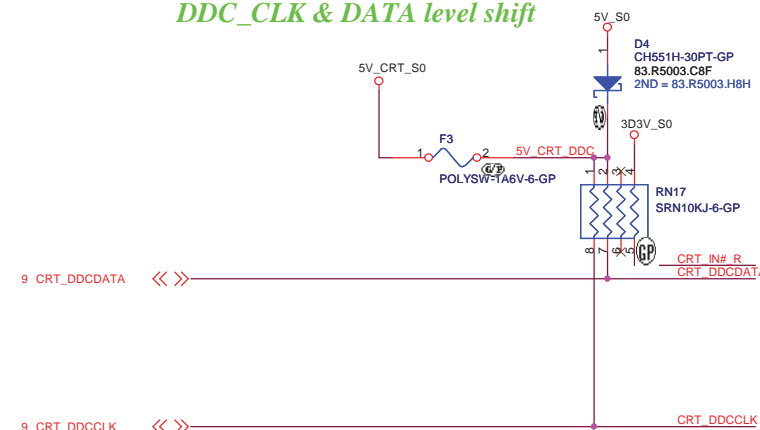
## CRT I/F & CONNECTOR



## Hsync & Vsync level shift



## DDC\_CLK & DATA level shift

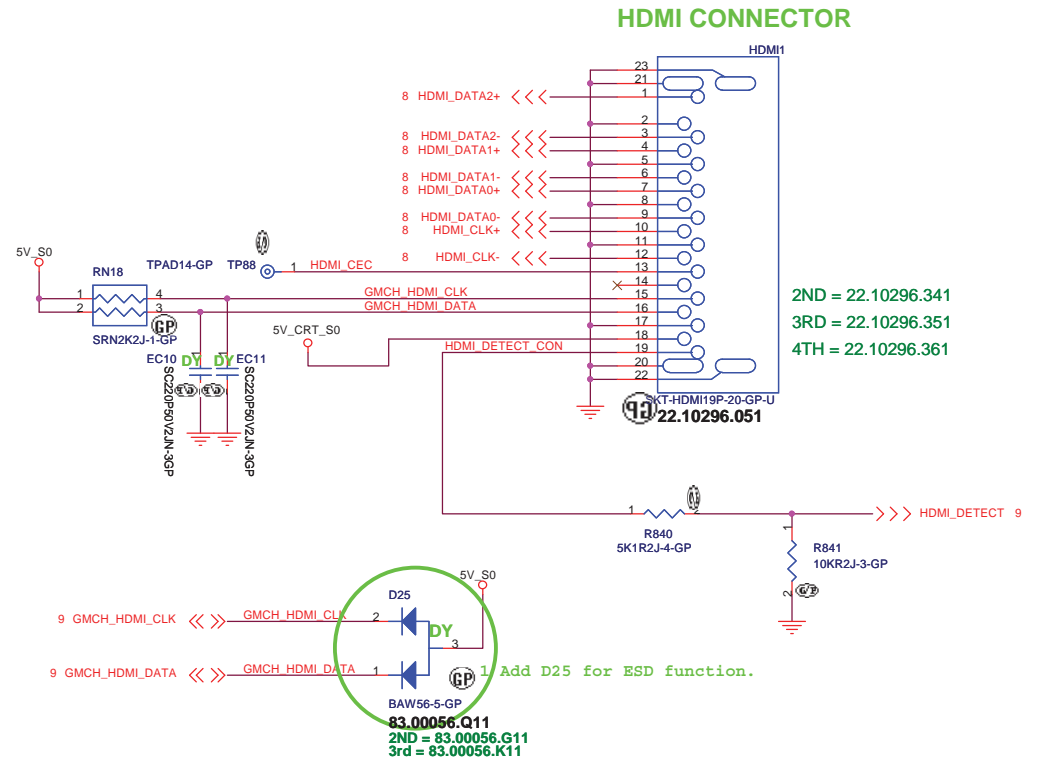
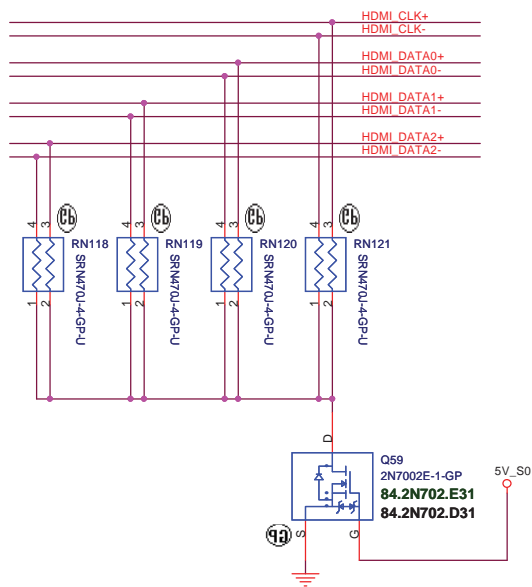


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Taipei Hsien 221, Taiwan, R.O.C.

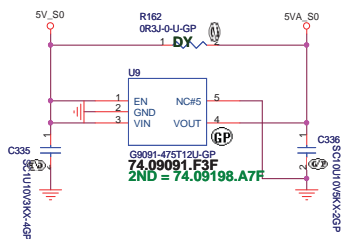
Title		CRT conn	
Size	Document Number	SJV10-NL	
A3		Rev -1	
Date:	Tuesday, January 26, 2010	Sheet 20	of 42



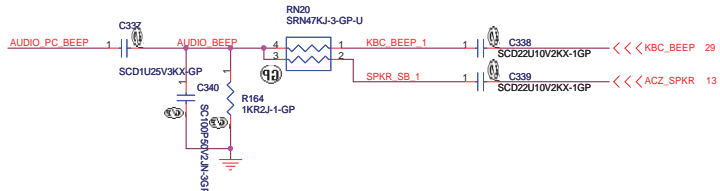


SJV10-NL

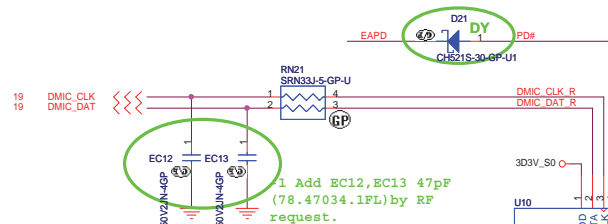
<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title HDMI conn</b>	
<b>Size A3</b>	<b>Document Number SJV10-NL</b>
<b>Date: Tuesday, February 02, 2010</b>	<b>Rev -1</b>
<b>Sheet 21</b>	<b>of 42</b>



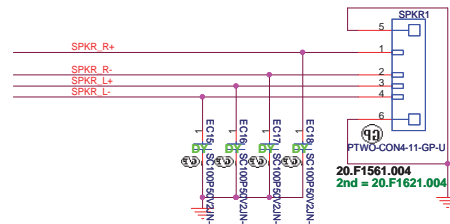
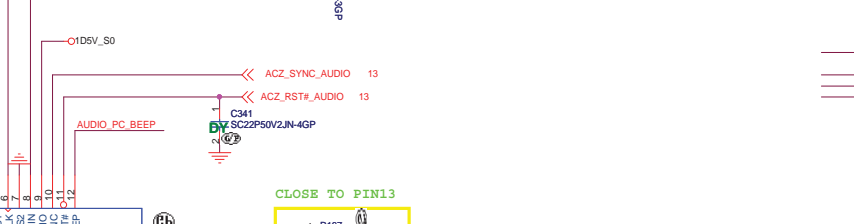
13 ACZ\_SDATAIN0 <<< R165 10R2J-2-GP <<< ACZ\_SYNC\_AUDIO 13  
13 ACZ\_BITCLK\_AUDIO >>>  
13 ACZ\_SDATAOUT\_AUDIO >>>  
-1 Change R166 to reserved D21.



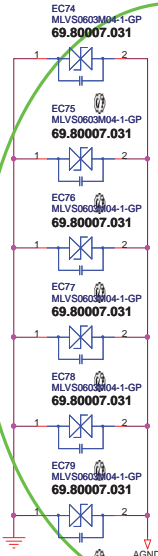
Internal Speaker



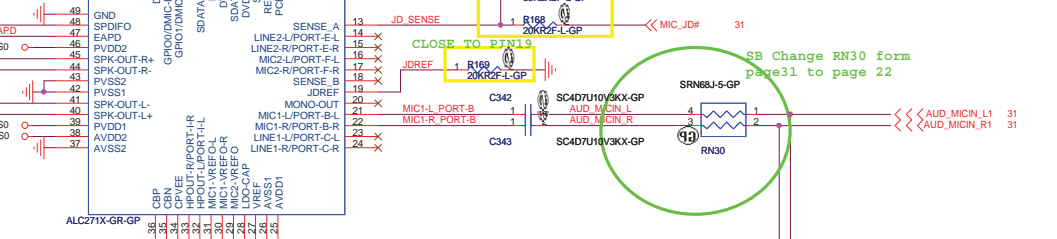
1 Add EC12, EC13 47pF (78.47034.1PL) by RF request.



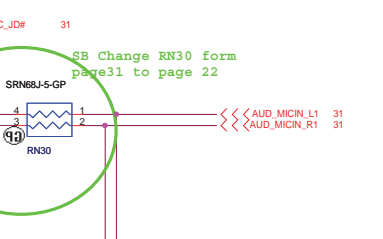
20.F1561.004 2nd = 20.F1621.004



-1 Add R335, EC74-EC79 for AGND connect.



SB Change C344 from 10uF to 0.1uF for anti pop noise.

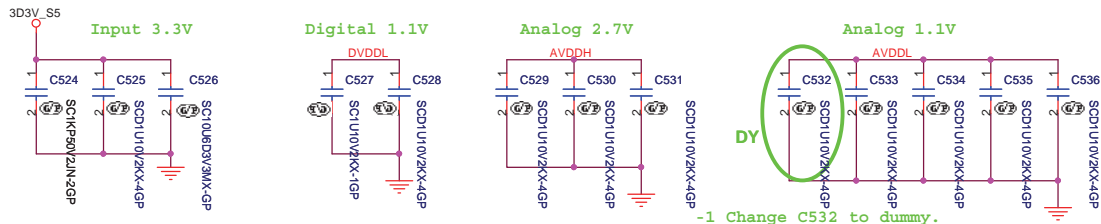


SJV10-NL

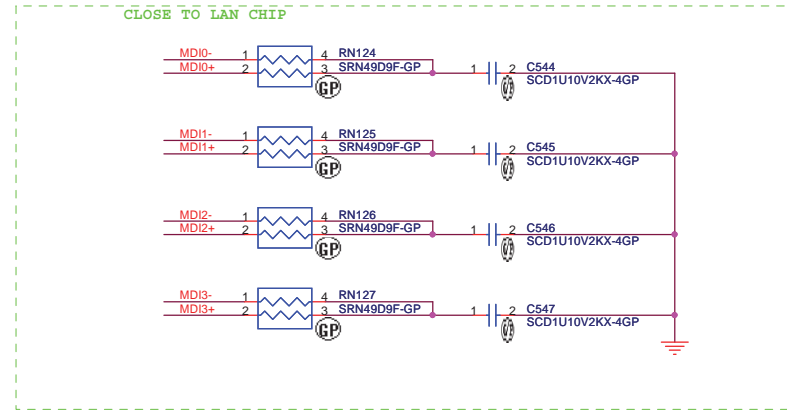
緯創資通 Wistron Corporation  
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Title			AUDIO_ALC271
Size	Document Number	SJV10-NL	
Custom			Rev -1
Date: Friday, January 28, 2010		Sheet 22	of 42

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-1 Change C532 to dummy.

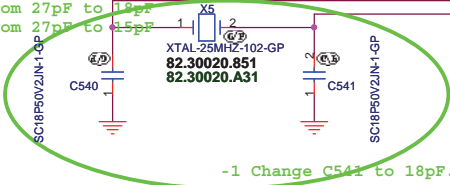


-1 Add reserved R875, change pull high to 3D3V\_S5.

3 LAN\_CLKREQ# <<< 1 2 LAN8151\_CLKREQ#

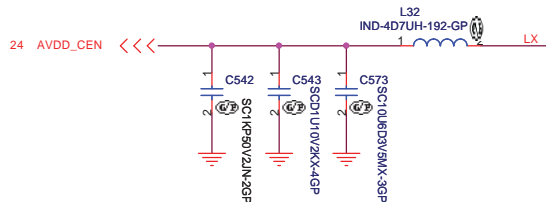
12.26 PCIE\_RST#\_R >>> 13.26 PCIE\_WAKE# <<< LAN8151\_CLKREQ#

SB 2nd source change from 82.30005.C51 to 82.30020.A31  
Change C540 from 27pF to 18pF  
Change C541 from 27pF to 15pF



-1 Change C541 to 18pF.

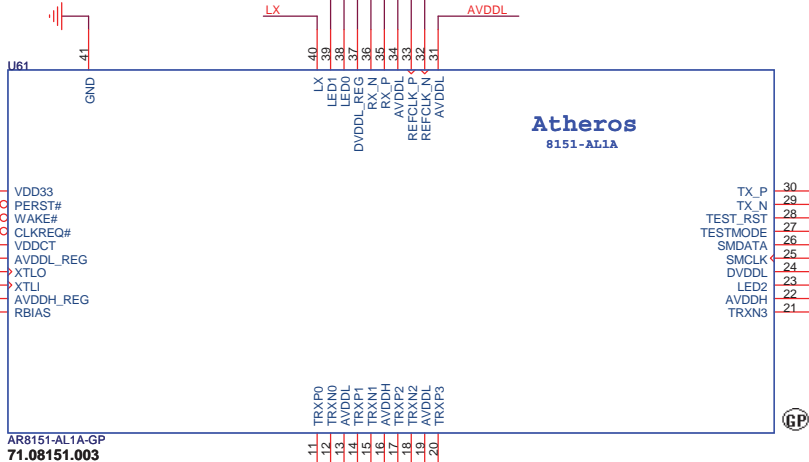
Analog 1.7V



公板LED1 Link LED0 Active

8 PCIE\_TXP1 8 PCIE\_TXN1 >>> <<< CLK\_PCIE\_LAN# 3 <<< CLK\_PCIE\_LAN# 3

24 LAN\_ACT\_LED# <<< 24 10M/100M/1G\_LED# <<< check



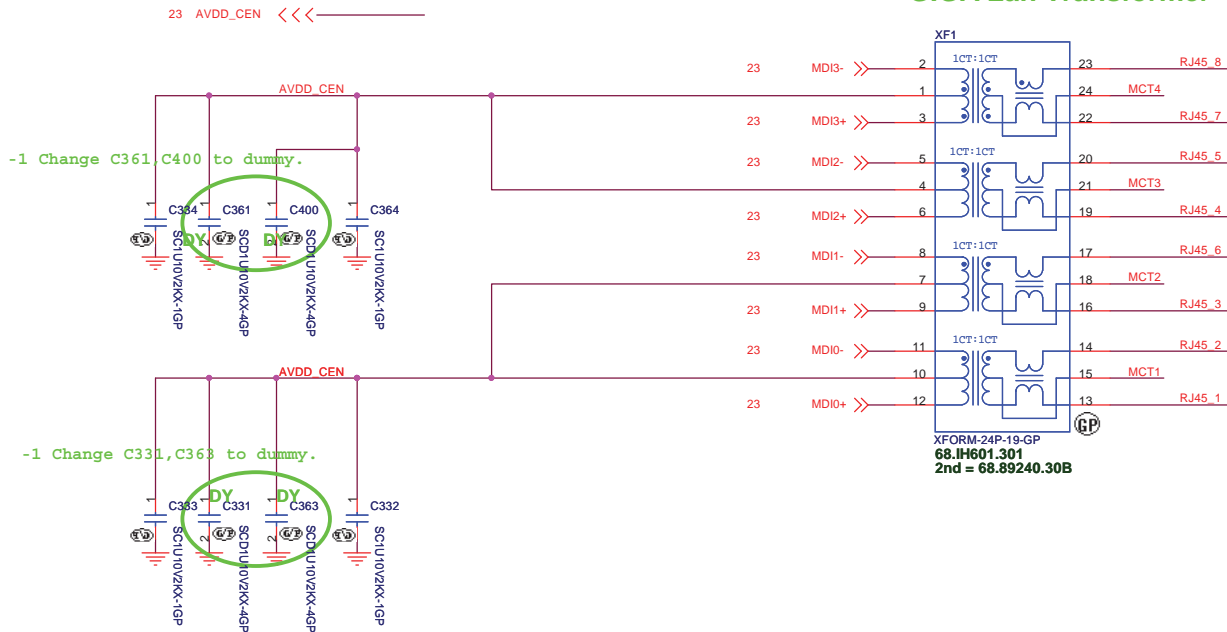
24 MDIO+ <<< 24 MDIO- <<< 24 MDI1+ <<< 24 MDI1- <<< 24 MDI2+ <<< 24 MDI2- <<<

>>> MDI3+ 24

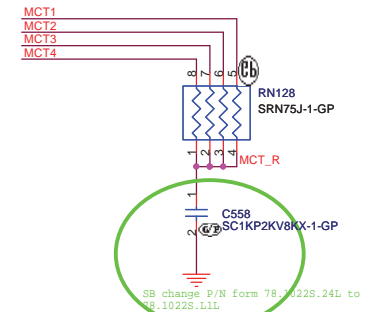
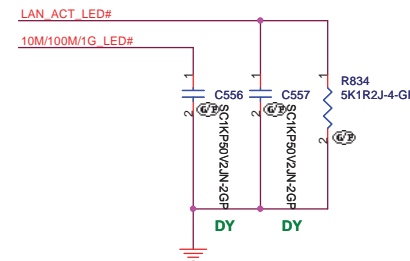
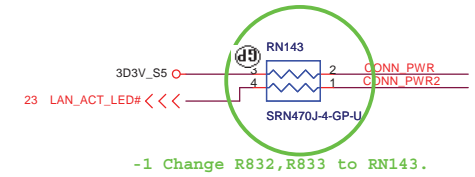
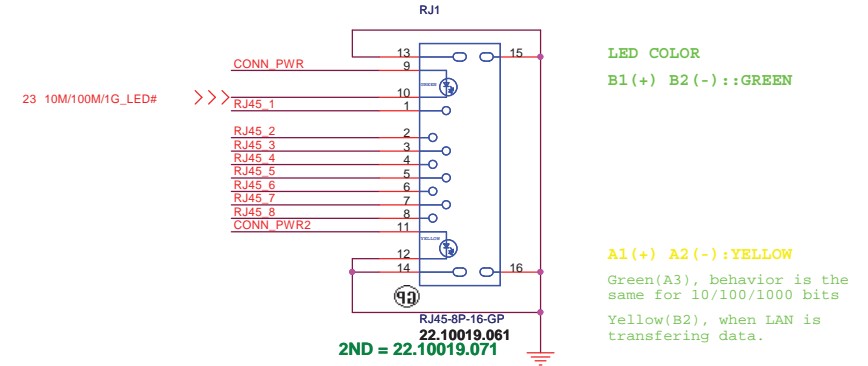
SJV10-NL

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

## Change 單顆 GIGA Lan Transformer



## LAN Connector



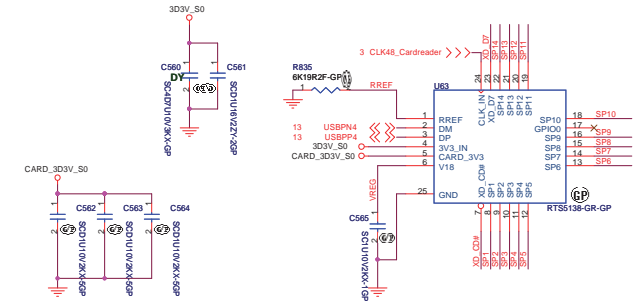
SJV10-NL

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Title		
LAN CONN		
Size	Document Number	Rev
A3	SJV10-NL	-1
Date: Tuesday, January 26, 2010		Sheet 24 of 42

## 5 IN1 CARD-READER



SB change P/N to 20.10087.011

-1 change Card1 P/N to 62.10024.B41



KBC

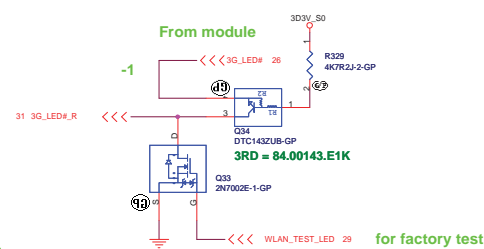


LED Always On  
WLAN\_LED Low  
WLAN\_TEST\_LED High

Factory test use  
WLAN\_TEST\_LED High

-1 Change 3G LED portion circuit

From module

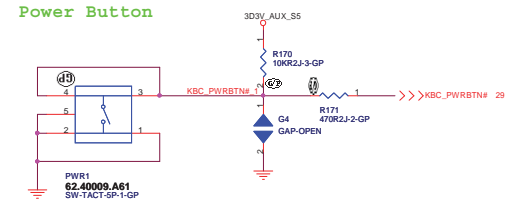


for factory test

## Power Button

[illegible]

HDD LED  
(BLUE)



SJV10-NL

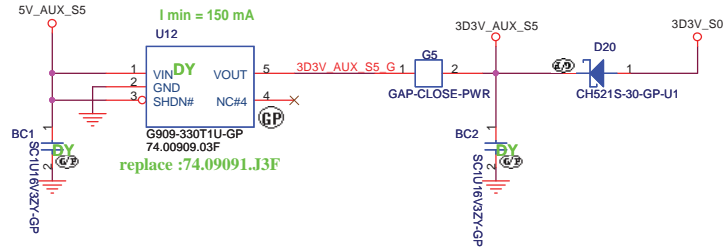
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Taipei Hsien 221, Taiwan, R.O.C.

Title				<b>LED_CARD reader</b>			
Size A2		Document Number				Rev	
		<b>SJV10-NL</b>				<b>-1</b>	
Date: Monday, February 01, 2010				Sheet 25 of		42	

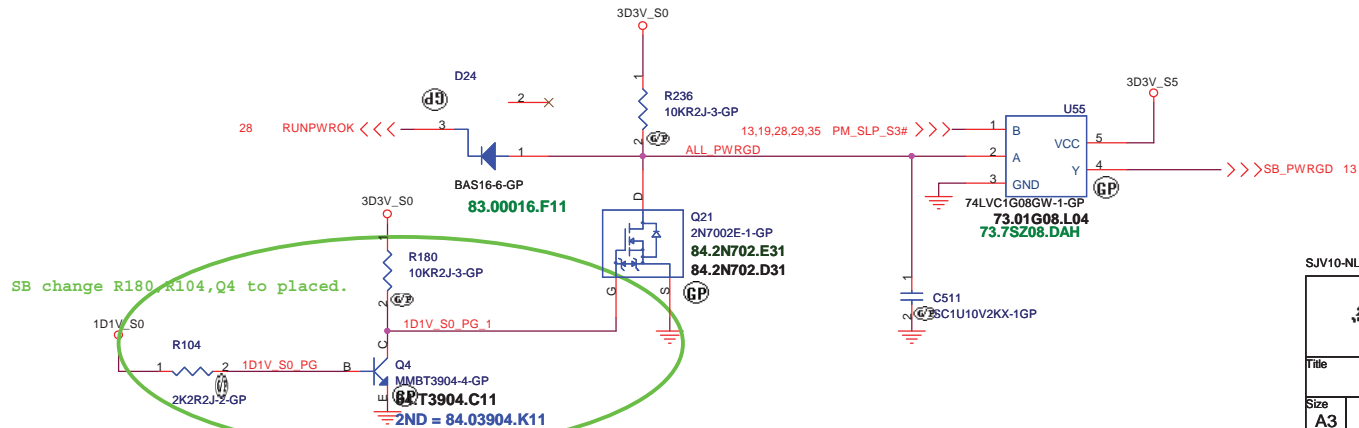
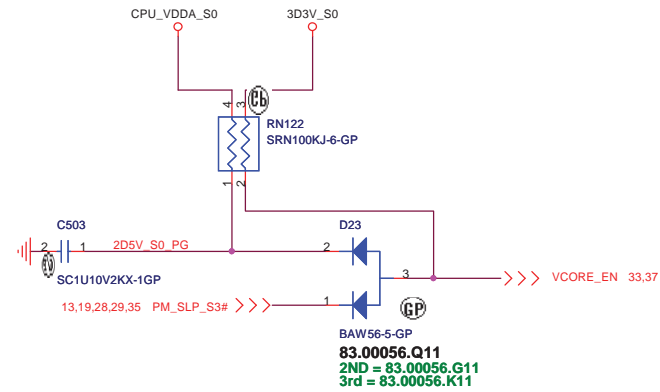
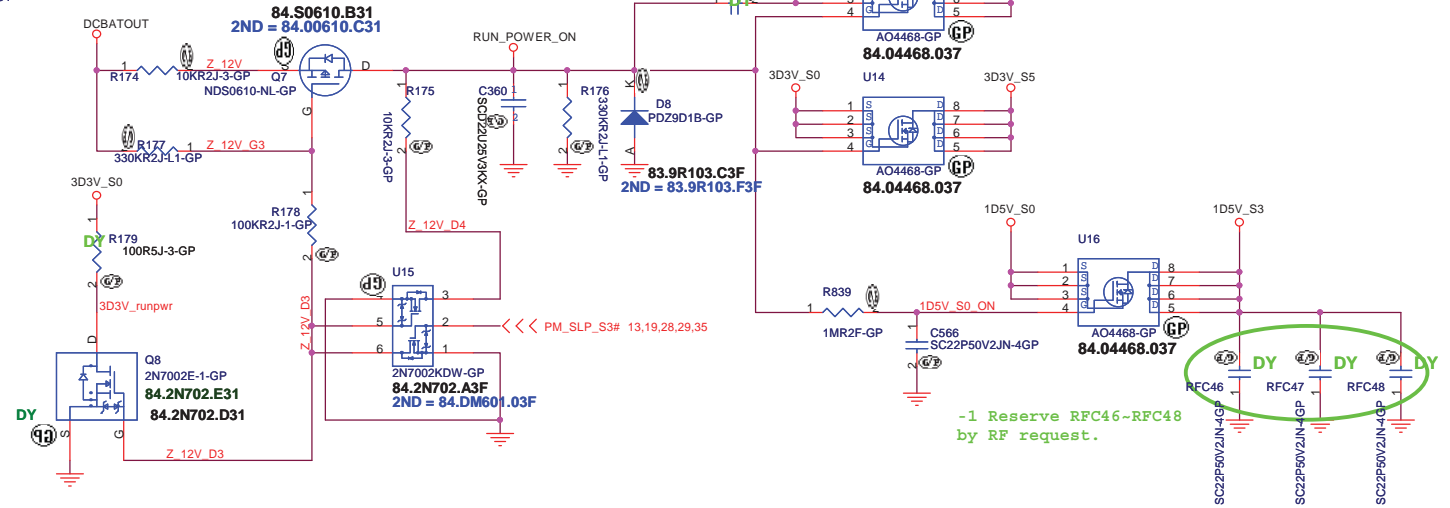




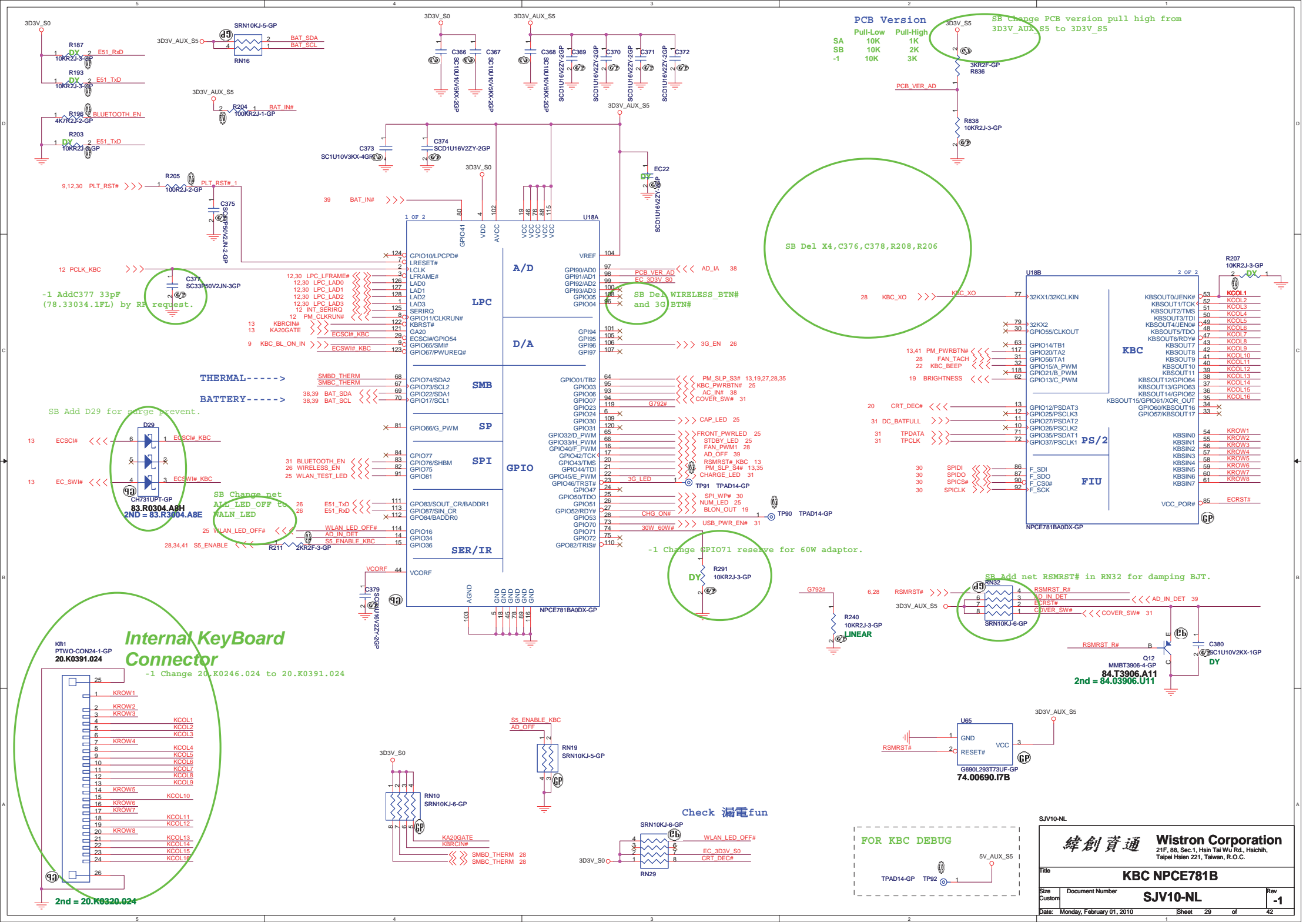
# Aux Power 3D3V\_AUX\_S5



# Run Power

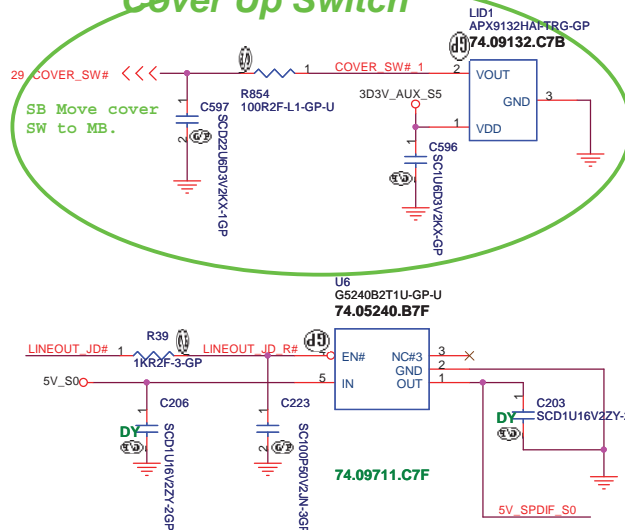




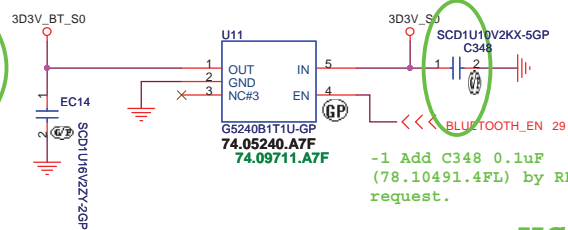




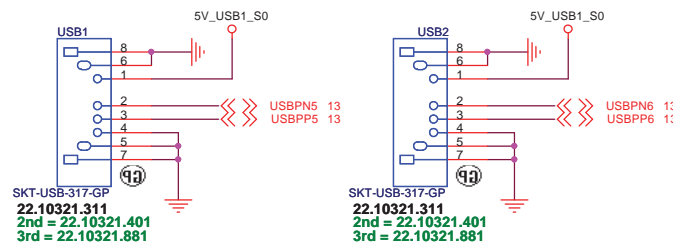
## Cover Up Switch



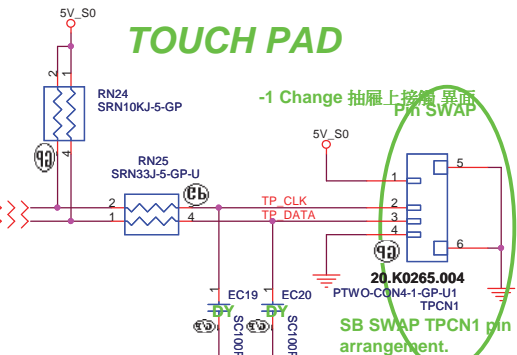
## BLUETOOTH MODULE



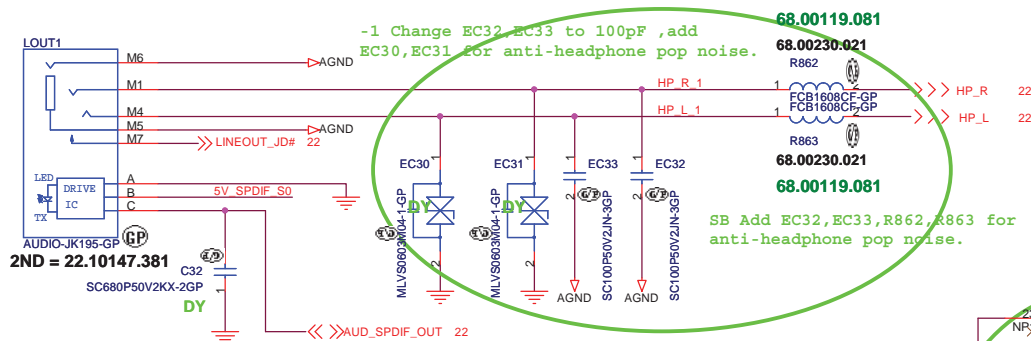
## USB MODULE



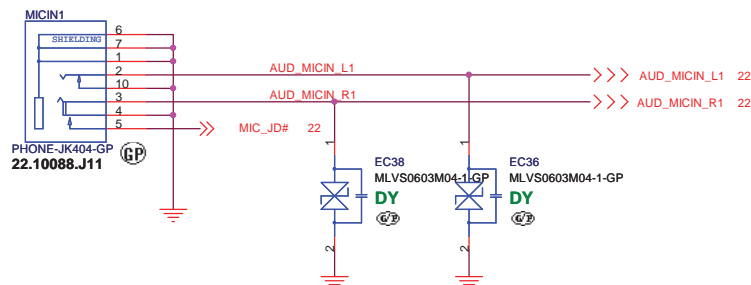
## TOUCH PAD



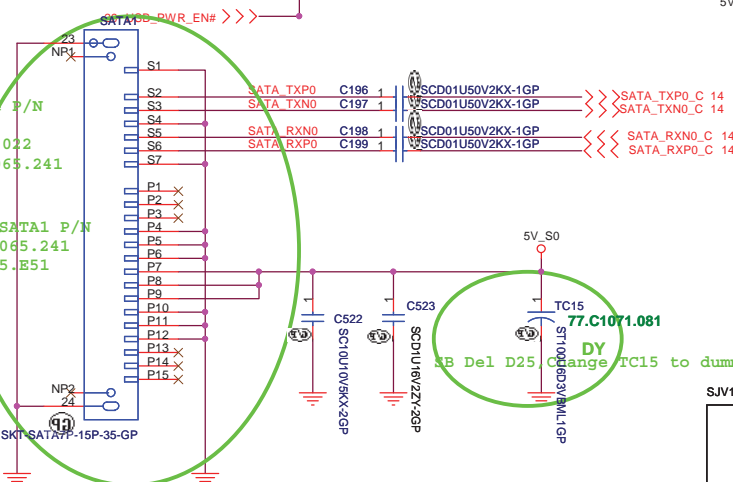
## LINE OUT 不要選用有鐵殼的



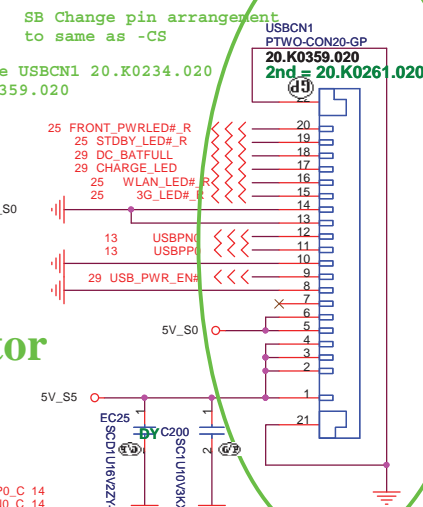
## MIC IN change 22.10088.I71



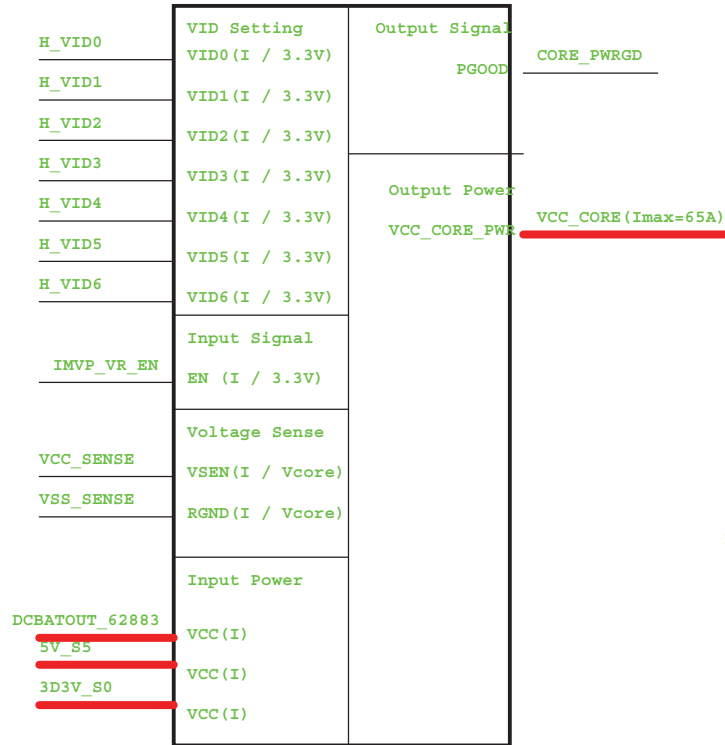
## SATA Connector



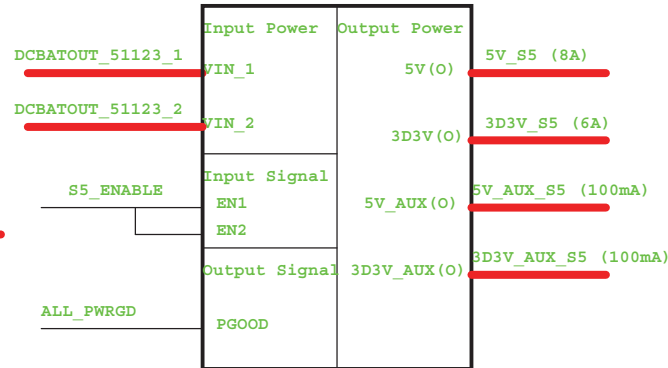
## USB Connector



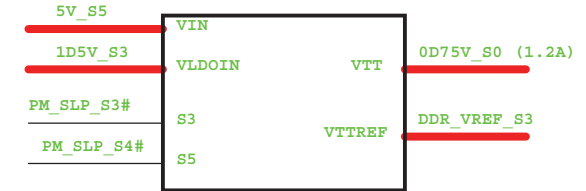
### ISL62883 VCC\_CORE



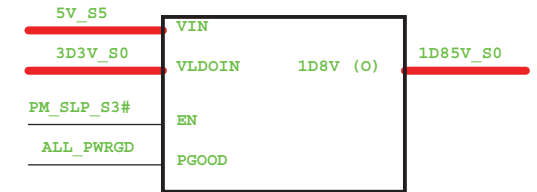
### TPS51123 5V/3D3V



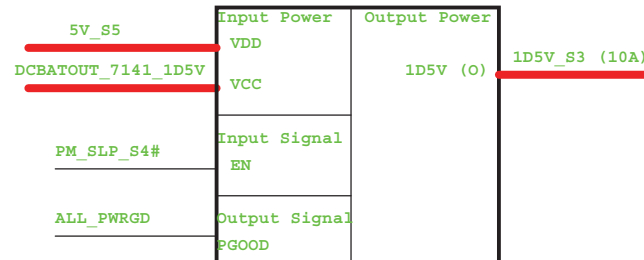
### RT9026 0D75V\_S0



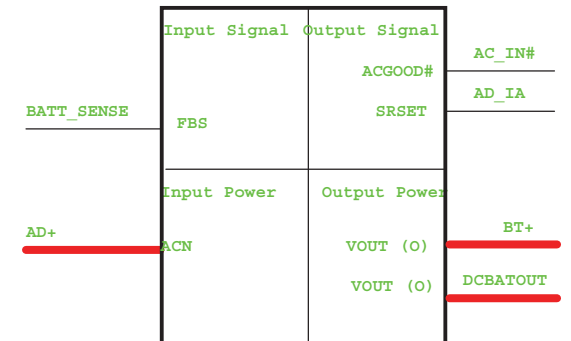
### RT9025 1D8V



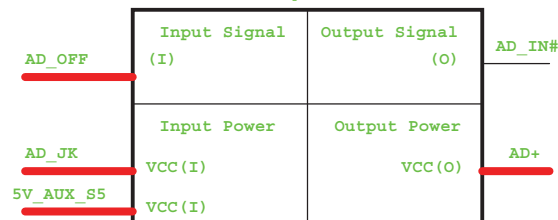
### RT9025 1D5V



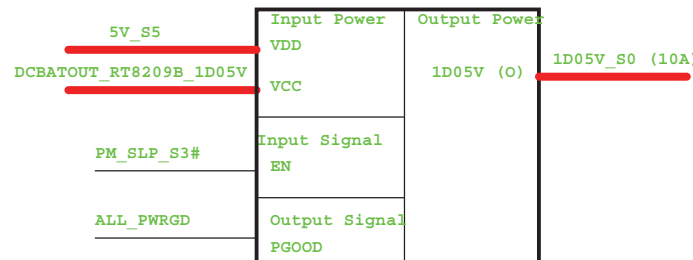
### Charger BQ24745



### Adapter



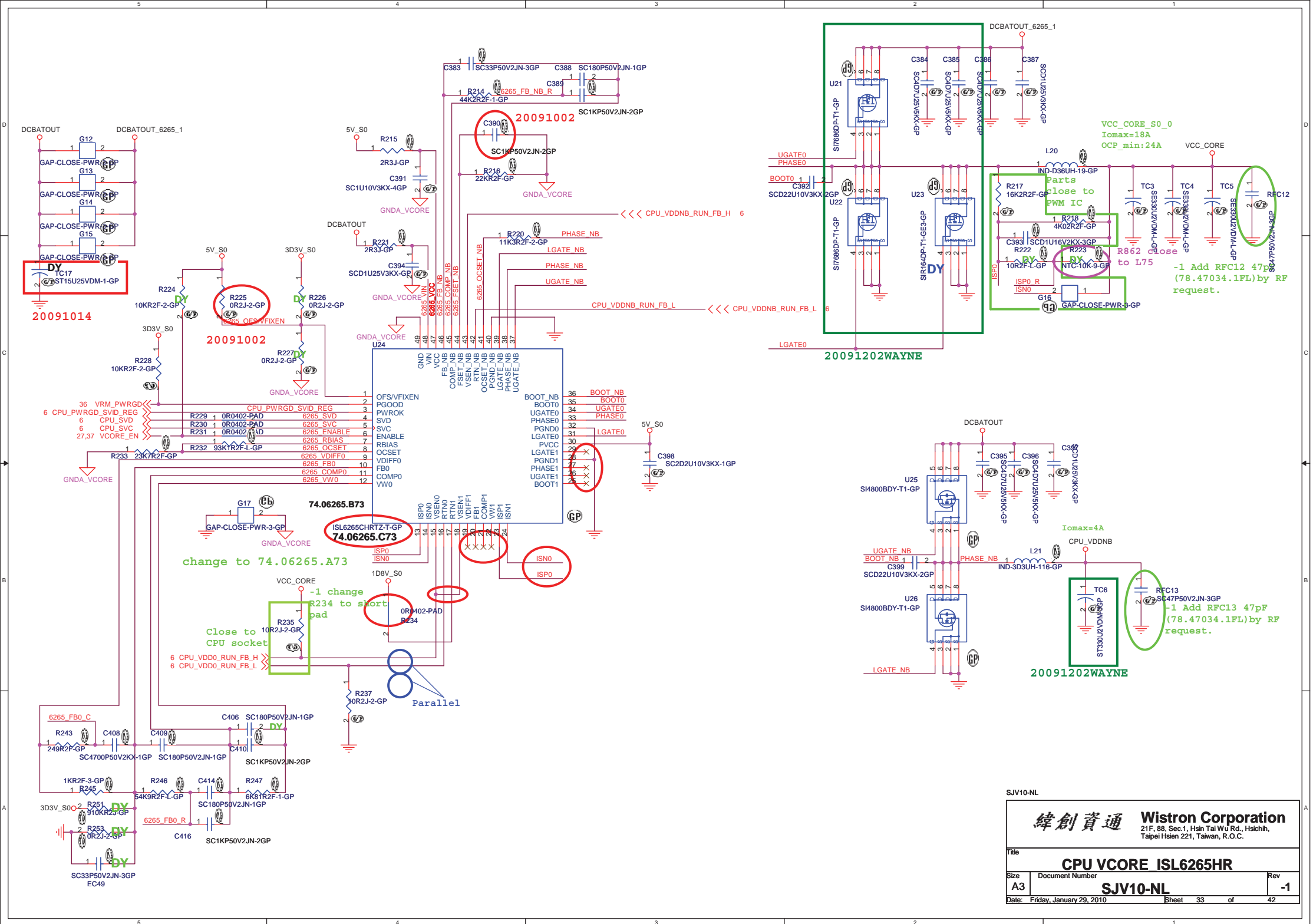
### RT8209B 1D05V



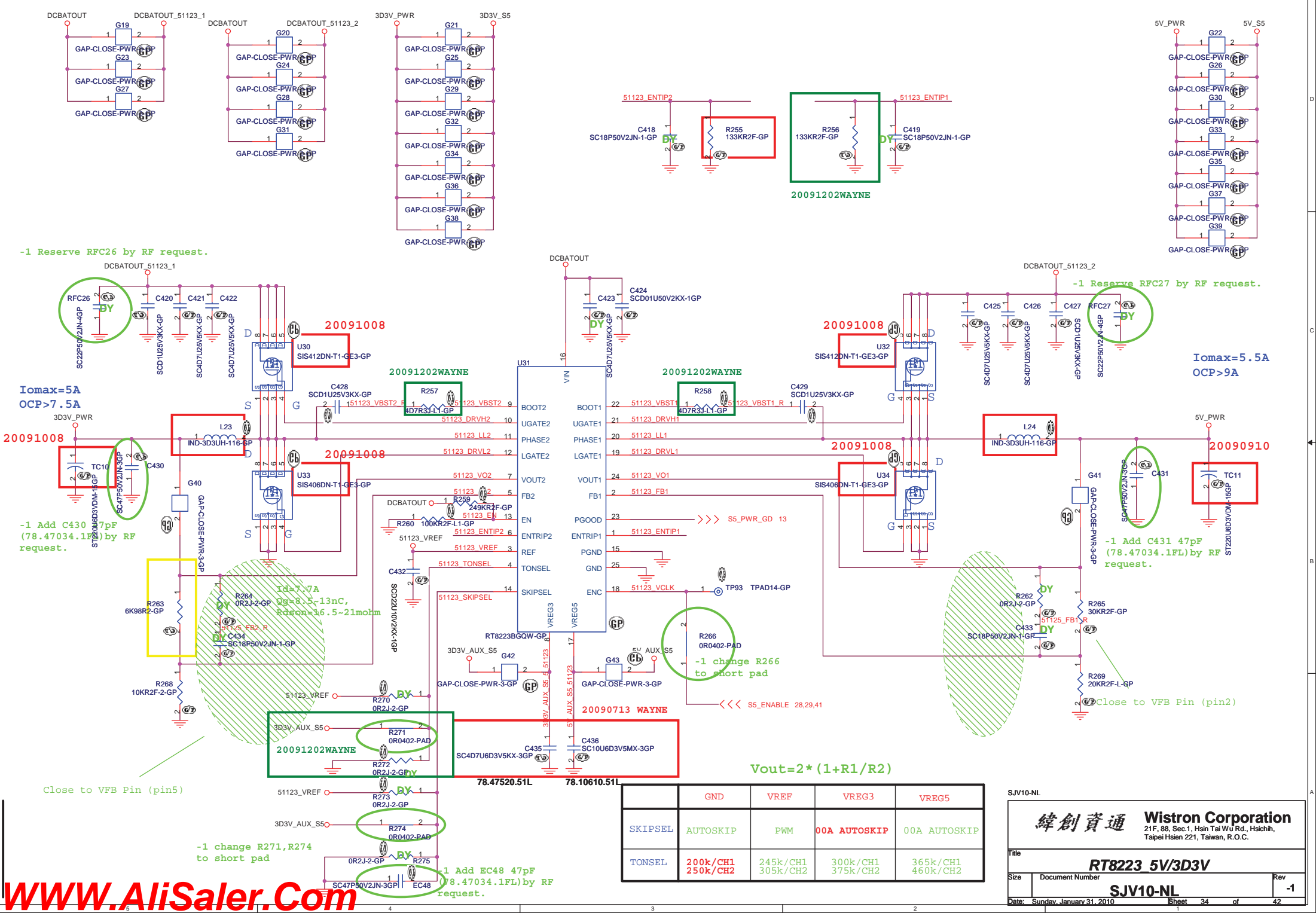
SJV10-NL

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Title			
Power Block Diagram			
Size	Document Number	Rev	
	SJV10-NL	-1	
Date:	Tuesday, January 05, 2010	Sheet	32 of 42







	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

緯創資通

Wistron Corporation

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File

RT8223 5V/3D3V

Size

Document Number

Rev

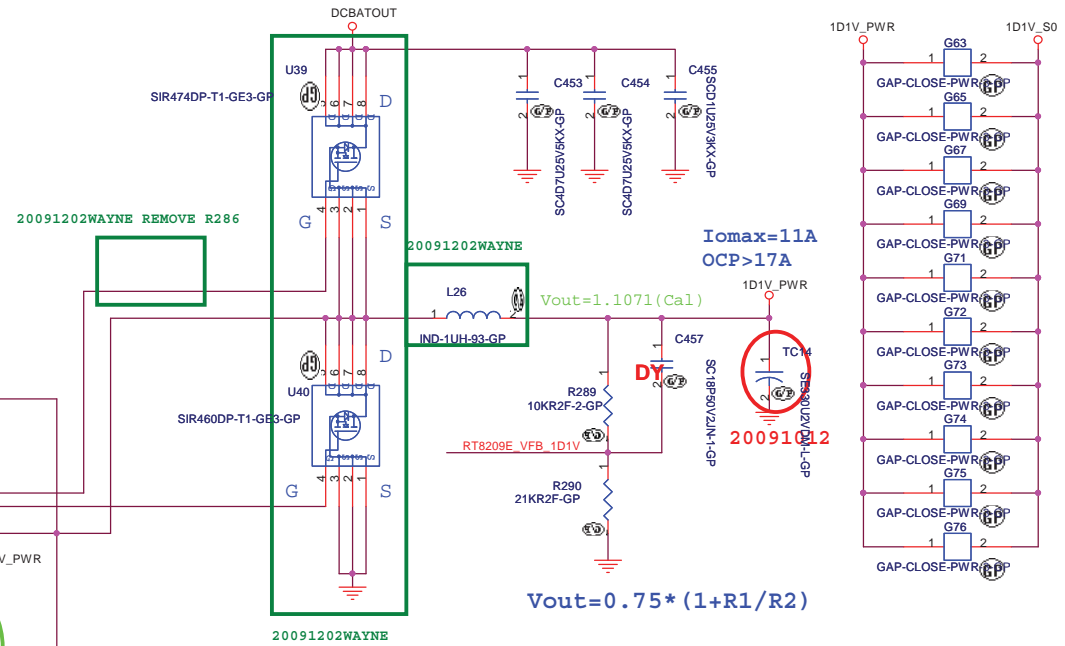
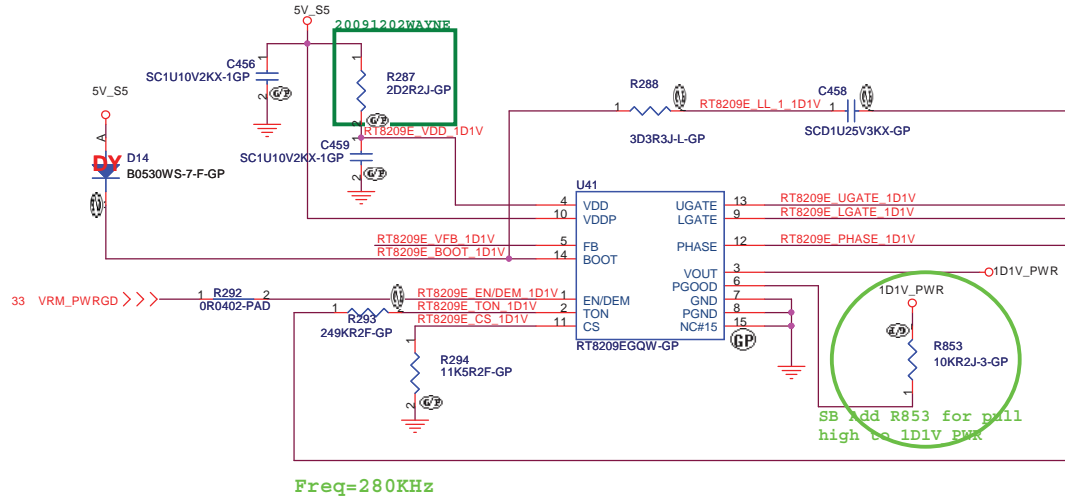
-1

Date: Sunday, January 31, 2010

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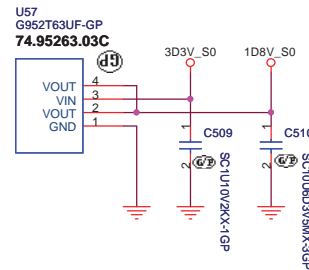


## RT8209E for 1D1V\_S5



## 1.8V\_S0

## 1.8V 1A Regulator



0921

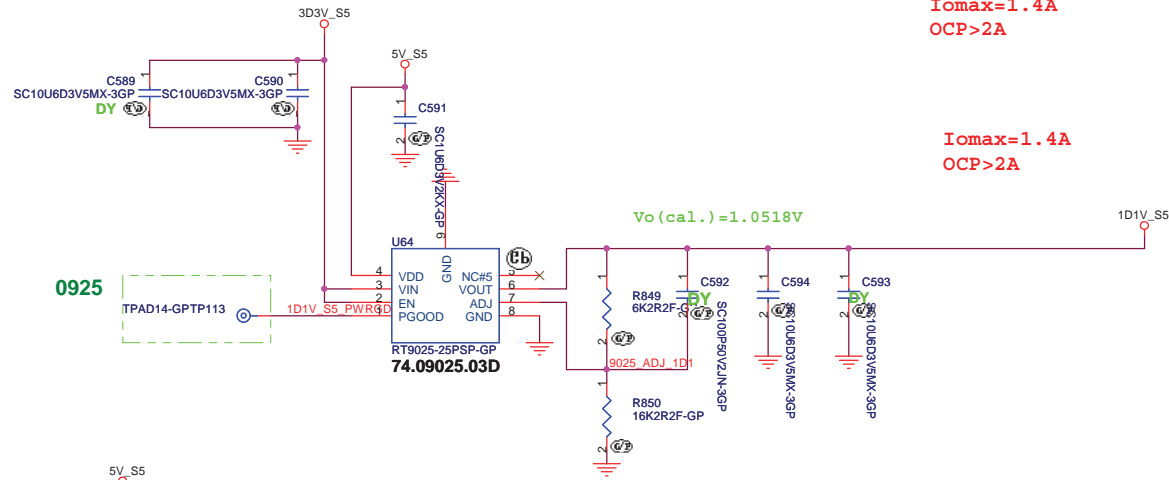
## RT9025 for 1D1V\_S5

$I_{\text{omax}}=1.4\text{A}$   
 $\text{OCP}>2\text{A}$

$I_{\text{omax}}=1.4\text{A}$   
 $\text{OCP}>2\text{A}$

 $V_o(\text{cal.})=1.0518\text{V}$ 

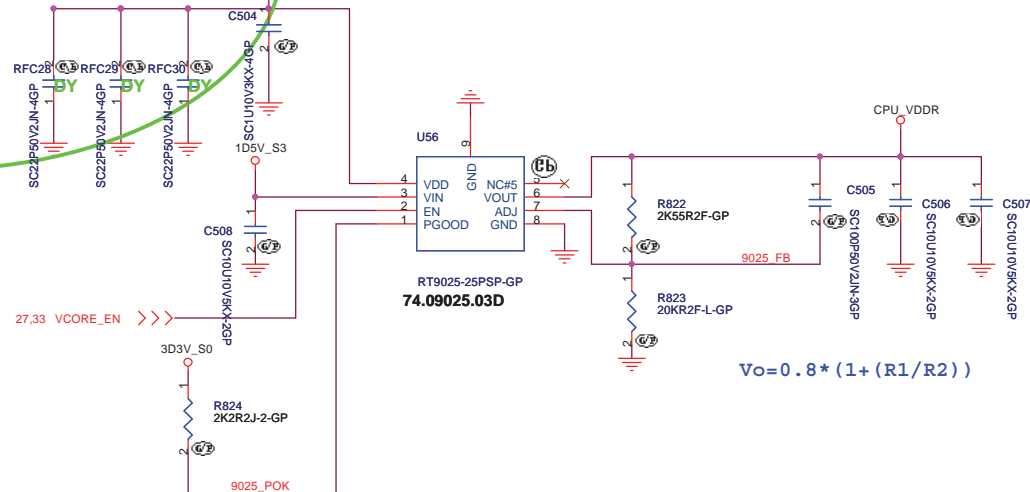
0925



$$V_o = 0.8 * ((R1+R2) / R2)$$

$$= 0.8 * ((6.2\text{K}+16.2\text{K}) / 16.2\text{K}) = 1.106\text{V}$$

-1 Reserve RFC28~RFC30, RFC37~RFC42, RFC44, RFC45 by RF request.



$$V_o = 0.8 * (1 + (R1/R2))$$

SJV10-NL

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Title

**LDO 1D5 S0 0D9 S0**

Size  
A3

Document Number

**SJV10-NL**

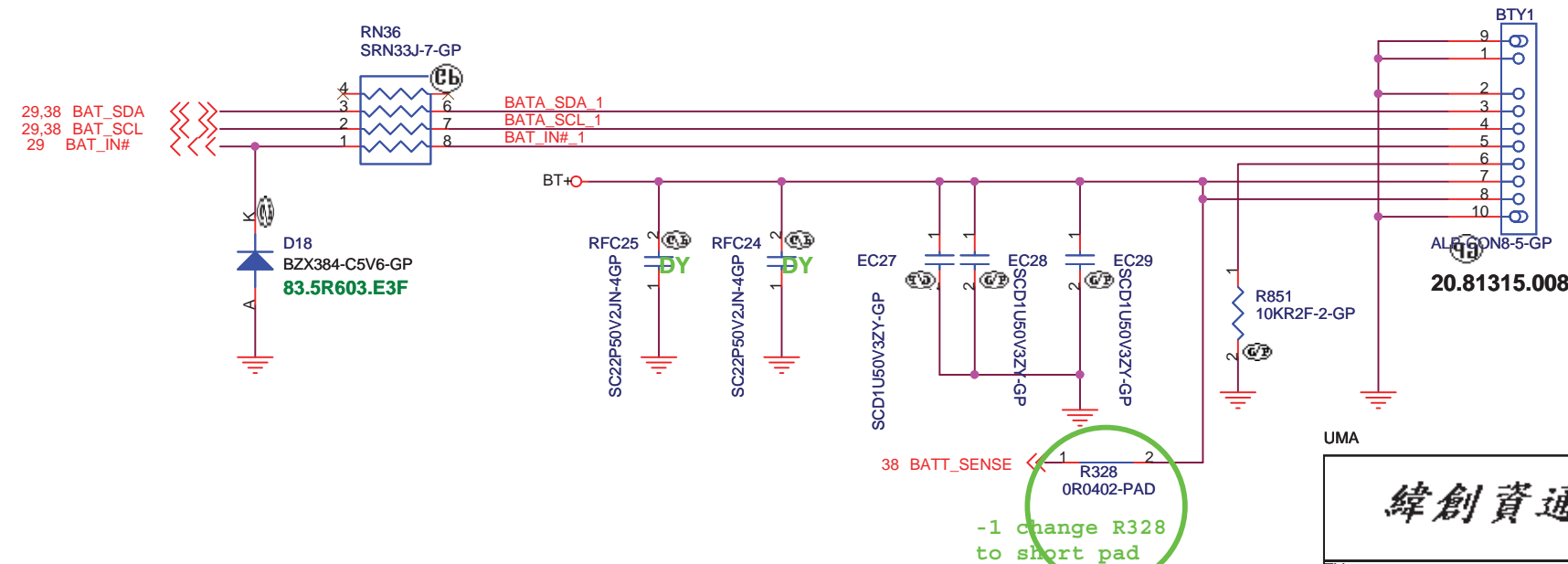
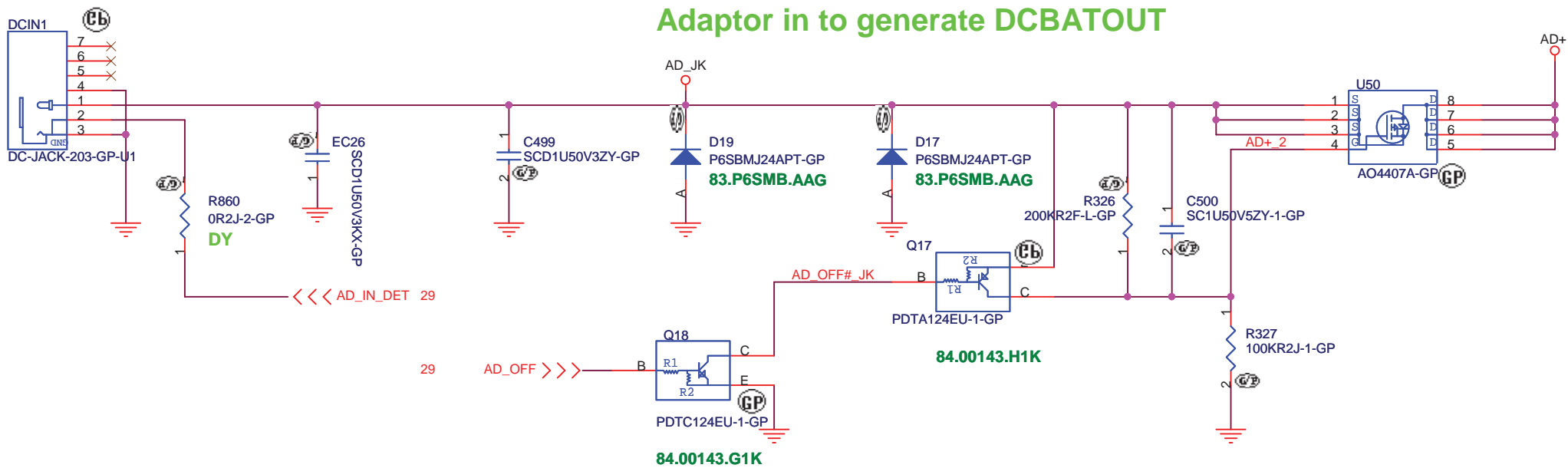
Rev

**-1**

Date: Sunday, January 31, 2010

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UMA

緯創資通

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Title

**AD / BATT CONN**

Size

Document Number

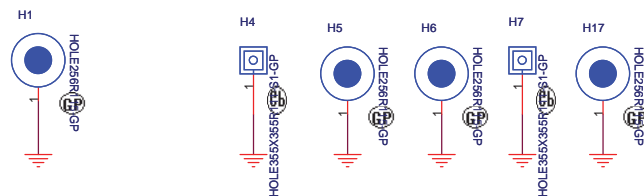
**SJV10-NL**

Rev

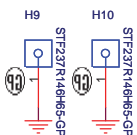
-1

Date: Saturday, January 30, 2010

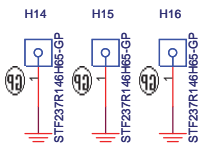
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**MB HOLE**



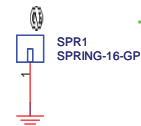
**MINI CARD BOSS**



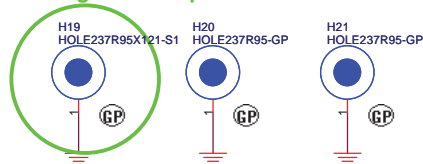
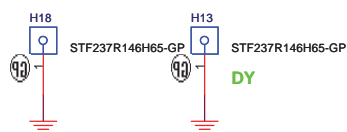
**CPU NB BOSS**

**SPRING**

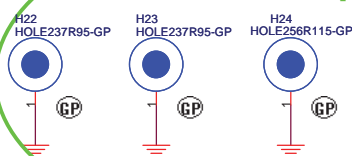
-1 Add SPR1 for RTC battery.



-1 Change H19 shape



SB Add H22,H23,H24 for ME request.



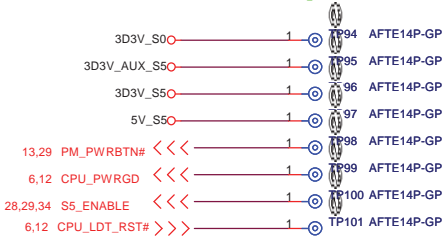
SJV10-NL

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
<b>EMI/Spring/Boss</b>		
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Date: Wednesday, January 27, 2010	Sheet 40 of 42	



Check test point



Test Point放在Dimm Door打開可量測處

SJV10-NL

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Title			
AFTE_TP			
Size	Document Number		Rev
	SJV10-NL		-1
Date:	Tuesday, January 26, 2010		Sheet 41 of 42

SB Change notice:  
1. Change C344 from 10uF to 0.1uF for anti pop noise.(Page 22)  
2. ChangeU48 circuit from 74.88731.C73 to 74.88731.B73 ,(SA BOM already 74.88731.B73 used.).(Page 38)  
3. SWAP TPCN1pin arrangement.(Page 31)  
4. Change U19 to 2MB(72.25165.A01, 72.25016.A01).(Page 30)  
5. X1 need to change to the same as JV10-CS (82.30005.A51).(Page 3)  
6. Del X4,C376,C378,R208,R206 ,R829 change to placed.(Page 28,29)  
7. Add G122 (Page 12).  
8. Add net RSMRST# in RN32 for damping BJT.(Page 29)  
9. X5 2nd source change from 82.30005.C51 to 82.30020.A31,Change C540 from 27pF to 18pF,Change C541 from 27pF to 15pF (page28)  
10. R272 change to dummy.(Page 34)  
11. Change R43 from Dummy to 1M ohm.(Page 12)  
12. Del R285, Add R852,R853 for pull high to 1D1V\_PWR and 1D5V\_PWR.(Page 35,36)  
13. Change RN30 form page31 to page 22.  
14. Add D28 for thermal trigger S5 shutdown.(Page 28)  
15. Del net RSMRST#\_SB pull high , Change S5\_PWR\_GD pull high from R261 to RN43.(Page 13)  
16. Change pin arrangement to same as ~CS, move cover SW to MB,Del WIRELESS\_BTN# and 3G\_BTN#. (Page 29,31)  
17. Change PCB version pull high from 3D3V\_AUX\_S5 to 3D3V\_S5,R836 1K change to 2K (page29).  
18. Change GPIO16 net name from ALL\_LED\_OFF to WLAN\_LED .(page29)  
19. Change C558 1000pF P/N form 78.1022S.24L to 78.1022S.L1L.(page24)  
20. Change capacity from 6.8pF (78.6R864.1FL) to 5.6pF (78.5R674.1FL)(page20).  
21. Change net PCLK\_FWH to LPCCLK0\_R change net PCLK\_KBC to LPCCLK1\_R(page16).  
22. Change R180,R104,Q4 to placed(page27).  
23. Change P/N from 20.F1416.022 to 62.10065.241(page31).  
24. Add D29 for surge prevent.(page29).  
25. Change Mini card 3G pin41 from 5V\_S5 to NC.(page26).  
26. Add C598 for solve CRT flicker issue (page9).  
27. Change R859 from 150 ohm to 140 ohm (page20).  
28. Add H22,H23,H24 for ME request. (page40).  
29. Del net E51\_RxD ,E51\_TxD (page26).  
30. Change R71 from bead 470 ohm to RES 3.9 ohm(page9).  
31. Del D25.(page31).  
32. Add RTC charge circuit.(page12).  
33. EC42,EC43 requested by EMI placed.(page38).  
34. Change LCD1 P/N from 20.F1093.040 to 20.F1703.040(page19).  
35. Change net PM\_SLP\_S4# to PM\_SLP\_S3#.(page35).  
36. Add EC32,EC33,R862,R863 for anti-headphone pop noise.(page31)  
37. Change C189 to 22pF, C190 to 15pF.(page12)  
38. Change TC15 to dummy.(page31)

-1 change notices:  
1. Change R91,R92 to RN132,R27,R30 to RN133,R34~R36 to RN134.(Page 3)  
2. DY C35,C42,C80,Change C36,C43,C569,C79 to 22uF.(Page 7)  
3. Change R60,R62 to RN136.(Page 9)  
4. Change R84,R85 to RN137,R76,R78 to RN138,R22,R79 to RN139.DY C139,Change C140 to 22uF.(Page 10)  
5. Change R89,R88 to RN140.(Page 12)  
6. Change R133,R135,R136,R128 to RN141,R138,R139 to RN142.(Page 16)  
7. Change C266,C281 to dummy.(Page 17)  
8. Change C287,C293,C302 to dummy.(Page 18)  
9. Change R16 to short PAD.(Page 19)  
10. Change C532 to dummy.(Page 23)  
11. Change C331,C400,C361,C363 to dummy,change R832,R833 to RN143.(Page 24)  
12. Change C357 to dummy.(Page 26)  
13. Change R844,R847 to short pad.(Page 28)  
14. Add reserved R865, change pull high to 3D3V\_S5.(Page 23)  
15. Change 10u/25V(78.10622.51L)to 4.7u/25V(78.47522.51L)(Page 19)  
16. Change C483,C423,C487,C490,C491,C493. 10u/25V(78.10622.51L)to 4.7u/25V(78.47522.51L)(Page 34,38)  
17. Change USBNC1 20.K0234.020 to 20.K0359.020 (Page 31)  
18. Change KB1 20.K0246.024 to 20.K0391.024(Page 29)  
19. Change R234 to short pad.(Page 33)  
20. Change R266,R271,R274 to short pads.(Page 34)  
21. Change R328 to short pad.(Page 39)  
22. Change 3G LED portion circuit.(Page 26)  
23. Change R166 to reserved D21.(Page 22)  
24. Change 抽屜上接觸 異面.(Page 31)  
25. Add SPR1 for RTC battery.(Page 40)  
26. Add VRAM identify pins.(Page 12)  
27. Change EC32,EC33 to 100pF,add EC30,EC31 for anti-headphone pop noise(Page 31)  
28. Change GPIO71 reserve for 60W adaptor.(Page 29)  
29. Reserve EC47 for EMI issue.(Page 13)  
30. Change DB1 to test pads.(Page 30)  
31. Change C12,C20,C193 to 12pF,C541 to 18pF.(Page 3,12,23)  
32. Add R335,EC74~EC79 for AGND connect.(Page 22)  
33. Change Card1 P/N to 62.10024.B41(Page 25)  
34. Change 10u/25V(78.10622.51L)to 10u/16V(78.10621.52L)(Page 19)  
35. Change SATA1 P/N from 62.10065.241 to 62.10065.E51.(Page 31)  
36. Add F4,D25 for ESD function.(Page 21)  
37. Reserve C310,RFC1,RFC11,RFC14,RFC16~RFC19,RFC22,RFC24~RFC30,RFC37~RFC42,RFC44~RFC48 by RF request.(Page 3,18,19)  
38. Add EC4,EC12,EC13,C306 (22pF)by RF request. (Page 3,19,22)  
39. Change R1,R4,R7 to bead (68.00373.001).(Page 3)  
40. Add C309,C430,C431,RFC12,RFC13,EC48 47pF (78.47034.1FL)by RF request.(Page 19,33,34)  
41. Add C303,C348,EC45 0.1uF (78.10491.4FL) by RF request.(Page 19,31,38)  
42. Add RFC10,C310 1200pF (78.12234.2FL)by RF request.(Page 19)  
43. Add EC23,EC24 10pF (78.10034.1FL) by RF request.(Page 30)  
44. Add C377 33pF (78.33034.1FL) by RF request.(Page 29)  
45. Change C189 to 15pF.(Page 12)

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緯創資通

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